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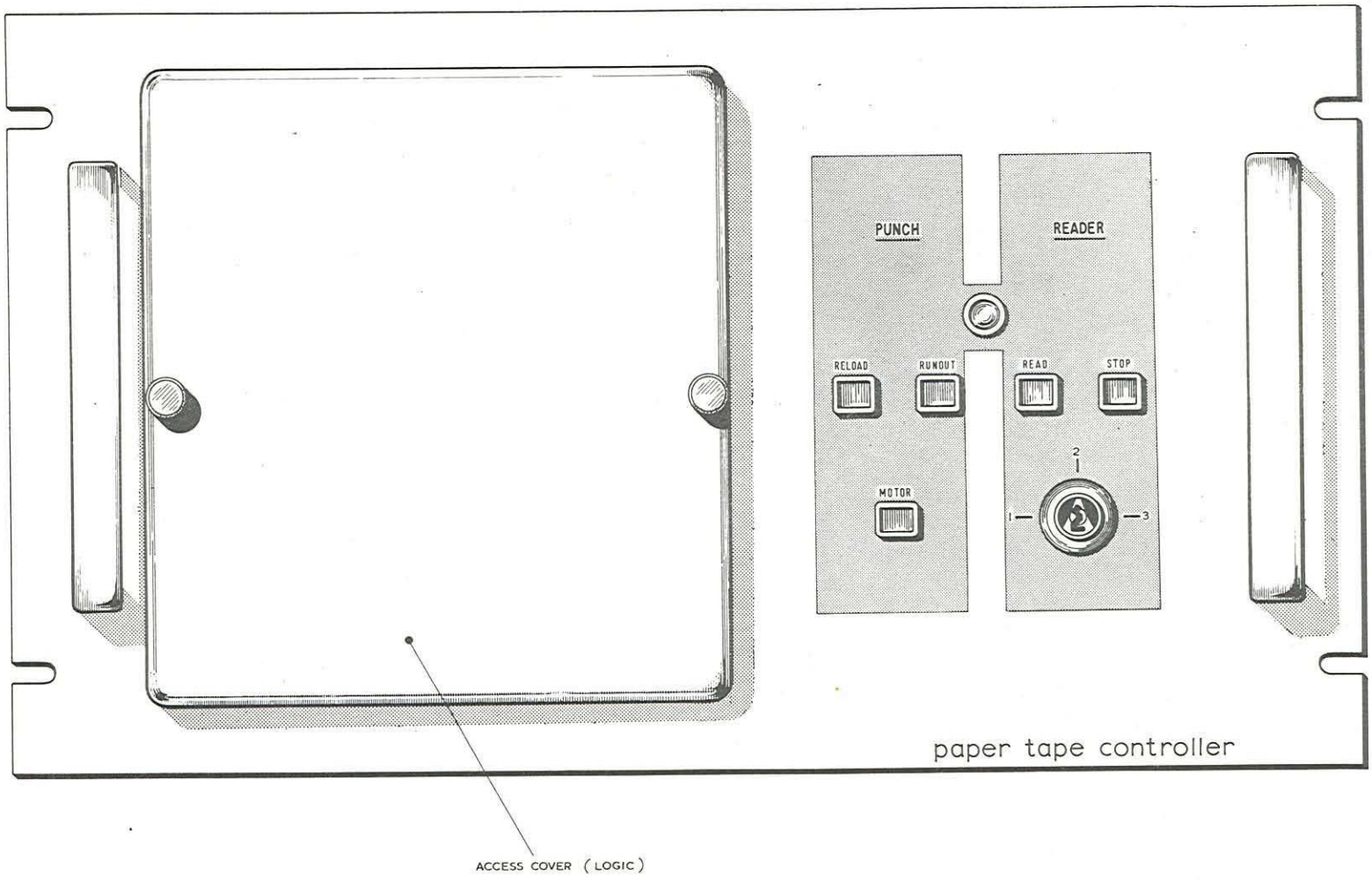

PAPER TAPE CONTROLLER, 19" RACK MOUNTING
STANDARD VERSION

(CAT. Nº MCB 60)

FIG. a

PAPER TAPE EQUIPMENT

1. GENERAL

Three types of paper tape equipment are current:

(i) Paper Tape Controller (MCB 60) with:
one Paper Tape Reader, 250 characters per second
(MCB 70)
or one Paper Tape Reader, 500 characters per second
(MCB 71)
and one Paper Tape Punch, 110 characters per second
(MCB 74)

(ii) Paper Tape Teleprinter Controller (MCB 66A)
(desk mounting)
or Paper Tape and Teleprinter Controller (MCB 66F),
(19in rack mounting) with:
one Paper Tape Reader, 250 characters per second,
with associated logic boards (MCB 66B).
and one Paper Tape Punch, 110 characters per second,
with associated logic boards (MCB 66C)
and/or one Teleprinter, stand and associated logic boards
(MCB 66D)

(iii) Program Loading Unit (MCB 62)

2. POWER SUPPLIES

Power supply units for the paper tape equipment associated with MCB 60 are as follows:

Paper tape power supply (MCB 30), 19in rack mounting

Input: 100-125V or 200-250V ±10%, 50 ± 1 c.p.s. mains

Output: 10V 3.5A a.c. (for reader lamp)
+10V 2.0A d.c.
-10V 0.75A d.c.
+28V 6.0A d.c.

alternative paper tape power supply (MCB 32)

Input: 100-125V or 200-250V ±10% 50-60 c.p.s. mains

Output: as MCB 30 except reader lamp is driven from +10V 3.5A d.c.

Details of these units appear in Part 4 (Power Supplies) of this Manual.

NOTE: The power supply unit for MCB 66 is included with catalogue items MCB 66A and MCB 66F, details of which are given in Part 3, Chapter 7.

3. INTERCONNECTIONS

Interconnections for the MCS 920B system are given in Fig. A1.

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PART 3: PAPER TAPE EQUIPMENT

CHAPTER 2: PAPER TAPE CONTROLLER MCB 60

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CHAPTER 2

PAPER TAPE CONTROLLER MCB 60

1. INTRODUCTION

The Paper Tape Controller MCB 60 enables the computer to be connected to:

One Tape Reader 250 ch/sec. (Elliott) MCB 70
or one Tape Reader 500 ch/sec. (Elliott) MCB 71
and one Tape Punch 110 ch/sec. (Teletype) MCB 74

The Paper Tape Controller contains the manual controls and circuits necessary for reading and punching paper tape of up to a maximum of eight tracks.

1.1 Tape Reader Control

Three modes of operation allow characters read from the tape to be interpreted according to the position of the TAPE READER MODE switch on the front panel of the unit. The switch is operated by means of a Yale-type key which may be removed from the unit when the mode of working has been selected.

The three modes are:

Mode 1. Seven bits are transmitted to the computer. Track five is ignored enabling eight track tapes punched in the Elliott/ 13. S. 3480 format (having the parity bit in track five) to be read without parity check.

NOTE: This code is also known as the 503/920A code.

Mode 2. Seven bits are transmitted to the computer as read from tracks one to seven inclusive, track eight is ignored. This enables eight track tapes punched in the A. S. C. I. I. /I. S. 0. format (with parity in track eight) to be read without parity check.

Mode 3. Eight bits are transmitted to the computer as read from tracks one to eight inclusive. This enables any tape format to be read by using a suitable program which may incorporate a parity check.

NOTE:- This code is also known as the 4100/903 code.

Five, six and seven track tape may be read in this mode, the state of the bits corresponding to unused tracks is undefined.

NOTE: Changes to the central processor are necessary if five, six or seven track tape is to be read under Initial Instruction.

The Tape Reader is buffered by an eight-digit register. The effect of a tape read instruction is to transmit the contents of this register to the computer and then to advance the tape to the next character. When the buffer register is loaded the tape movement is stopped when the leading edge of the next sprocket hole in the tape is detected.

1.2 Input Channel

The Tape Reader is connected to this channel and is selected by means of a 15 2048 instruction decoded by $\overline{P12}$, $\overline{P13}$.

Inputs from a tape source require a special routine to convert information from eight digit per character (seven information bits plus parity) paper tape to the 18 digit word computer standard. This is achieved in the central processor, Part 1, Chap. 4 refers.

1.3 Tape Punch Control

The computer instruction 15 6144 causes an eight bit character to be punched. If 5, 6 or 7 track tape is to be used, zeros must be transmitted to the unit in positions corresponding to the unused tracks.

Two manual controls are provided on the controller to govern the tape punch.

(i) RUN OUT button - causes the punch to feed blank tape

(ii) RE-LOAD button - incorporates a lamp which is lit when the " low tape " contacts on the punch operate . Once the contacts have operated, the lamp remains on. Computer instructions to the punch cannot be obeyed until the " low tape " condition has been cleared and the RE-LOAD button operated.

1.4 Output Channel

The Output channel is arranged for connection to a high speed paper tape punch. The eight least significant digit positions of the Accumulator being available for this purpose. Selection is by means of a 15 6144 instruction which allows the decode P13 P12 and $\overline{\text{P11}}$ of the tape punch.

1.5 Logic Circuits

The logic circuits of the Paper Tape Control are based on both the Elliott Minilog Logic elements featuring NOR logic and the LSA elements featuring NAND logic, Chap. 3 refers.

2. CONSTRUCTION

The logic circuits are contained on printed circuit boards with the following distribution:

Pos.	Qty.	Title	Function
1	1	A-FY	+6.0V d.c., 0, -6.0V d.c. Power Supply
2	1	A-AR3	Paper Tape Reader Control
3	1	A-AQ3	Paper Tape Reader Control (Selection and Reply)
4	1	A-AP3	Paper Tape Reader Register
5	1	A-FX	Receivers and Transmitters
6	1	$A\text{-}AO_3$	Paper Tape Punch Controls
7	1	A-AN3	Paper Tape Punch Controls
8	1	A-AM3	Paper Tape Punch Register
9	1	A-AK3	Paper Tape Punch Drivers

The logic of the Paper Tape Controller is depicted in Fig. C2.

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PART 3: PAPER TAPE EQUIPMENT

CHAPTER 3: CIRCUITS

CHAPTER 3

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CHAPTER 3

Circuits

1. GENERAL

The logic boards controlling read operations are:

A-AR_3 (Paper Tape Reader Control)

A-AQ_3 (Paper Tape Selection Control)

A-AP_3 (Paper Tape Reader Register)

The A-AR_3 and A-AQ_3 units exercise control over the mode of reader operation, originating the Reply Waveform, the drivers to the tape reader and clutch electromagnets in accordance with computer demand and/or waveforms from the Load Bar and Run-Out switch.

The A-AP_3 unit functions as an 8-bit buffer register between the tape reader and central processor.

Information between the Paper Tape Controller and central processor (data from the Tape Reader and for the Tape Punch together with control signals) is routed via cable receivers and transmitters on the A-FX unit.

These transmitters and receivers are constructed from LSAs and thus require +6V and -6V power supplies (as distinct from +10V and -10V supplies required for A-AR, A-AP and A-AQ units). The +6V and -6V supplies are obtained from the A-FY unit.

2. READER OPERATING SEQUENCE

2.1 Normal Cycle

During operation, the timing of the sequence is Asynchronous and is independent of the central processor.

2.1.1 Start Cycle

Assuming the Tape Reader has been loaded with tape and the read button operated, a tape input instruction from the computer results in

a Reader Select waveform, which signals the Paper Tape Controller. The Controller returns a Reply signal to the computer provided that a new character is available on the Input Reader lines.

The Reply signal cancels the Select waveform. This allows the computer to receive information from the Input Reader lines. This information will be the information taken from the tape under the reading head.

The effect of the Select waveform falling energises the clutch engage logic which moves the tape forward until the edge of the next sprocket hole is under the reading head. This then generates a sprocket waveform which after a delay period releases the clutch and with another delay, resets the Reader Register allowing the new information from the reading head to enter the register. It allows the next Select waveform to enter.

2.1.2 Last Cycle

If the central processor does not issue a data input instruction, the clutch is released. This stops the tape with the last character transferred one place past the reading position. The data from the holes under the reading head remain in the buffer until the next cycle transfer.

2.2 Sprocket Hole Waveforms

When the SPROCKET hole signal becomes false, a delay circuit is triggered; simultaneously the buffer register is reset. The delay period accommodates extreme skewing of the tape and worst case tolerances.

At the end of this period, a second pulse is triggered enabling the buffer to be loaded with the character. Sprocket hole waveforms are depicted in Fig. C2 (Sheet 2).

3. READER CONTROL (A-AR_3 and A-AQ_3 UNITS)

The logic of the Paper Tape Reader is given by Fig. C2 (Sheet 2). The conditional waveforms actuating this control set and reset bistables and/or switch elements in accordance with voltages originating at the control switches for the tape reader and by computer demand.

3.1 Reader Operating Conditions

With the tape reader under computer control, conditions prevailing at the A-AR_3 and A-AQ_3 units will be as follows:

(i) Select at +6.0V d.c.

(ii) Reader signal from the tape reader load switch +10.0V d.c.

(iii) IRS (initial reset) at 0 Volts. A C/R time constant followed by an inverter stage gives an initial positive pulse to reset the logic, afterwards it is maintained at 0 Volts when the 30 μF capacitor connected to the base of the IRS transistor has charged-up.

(iv) A R.O (Run-Out) signal of 0 Volts.

(v) Load bar (L.B) at 0 Volts.

(vi) Reply at +6.0 Volts.

(vii) Reader signal at 0 Volts.

The Error signal when produced, inhibits production of Reply, also lighting the lamp incorporated in the READ button on the Paper Tape Controller.

The NOR logic of the minilog elements will saturate when one or more inputs is at +10.0V inversion in the element giving an output pulse in the opposite sense. If all inputs are at less than 0.4 volt, the transistor will remain cut-off to give an output in the positive sense. Time relationships and pulse widths are determined by differentiator elements interposed between the elements of the logic chain.

3.2 Error

In the reader circuit of Fig. C2 (Sheet 2), an Error voltage will be generated initially on switching on until the Reader switch (READ button) has been operated. This action sets the reader bistable buffered by diodes D65/D66 with a +10.0 Volt signal applied through D65. The inverse output from this bistable falls to 0 Volts and a positive pulse is produced from the output of the following monostable. This output:

(a) Resets the ERROR bistable. This results in a 0 Volts ERROR output to permit the Reply to be produced, also extinguishing the Reader lamp on the Paper Tape Controller.

(b) Taken via a pulser and inverter to switch the final element in this chain giving a Reader output pulse of 10.0V d.c. which steps the tape one character.

3.3 REPLY

The REPLY waveform originates in the A-AQ_3 unit allowing a paper tape to be read in. At the initial switch-on, the IRS signal will set the bistable so that REPLY is inhibited. Operating the READ button will step the tape one character thus generating the $\overline{R/S}$ waveform. The $\overline{R/S}$ waveform is fed into the A-AQ_3 board where it resets the bistable so that as soon as SELECT appears, a REPLY is generated. When SELECT goes false again the monostable is triggered, the output of which is used to set the bistable so that REPLY is again inhibited until the tape has been stepped one character. The bistable will then be reset by $\overline{R/S}$. The bistable will also be set so that REPLY is inhibited if the ERROR signal is generated.

3.4. RUN-OUT

The RUN-OUT push button facilitates running tape at full

speed through the reader independently of the processor. When the button is operated the waveform RO is generated which is applied to the clutch logic circuits thereby engaging the clutch.

4. READER REGISTER (A-AP$_3$ UNIT)

The A-AP$_3$ Reader register functions as an eight digit buffer register accepting the output of the photo sensors of the paper tape reader. When loaded, (on detecting the leading edge of the next tape sprocket hole, a -6V signal), the contents of this buffer are transmitted to the computer by Reply going true.

The electrical output of the tape reader optical sensors is a function of the intensity of incident light so that each hole or blank generates a -6 Volt or 0 Volt waveform respectively, Fig. C5 refers.

The A-AP$_3$ register comprises eight bistable elements responding to an input of -6 Volts at one or more of the input Zener diodes. Where a code input is detected, a signal level of approximately 0 Volts is applied to the Code element and the resulting inverted output at +10 Volts is used to set the relative code bistable. An output of +10 Volts (or logic '1') will be obtained in this condition, which is routed via the A-FX unit to the receiver feeding the corresponding digit position in the G-register of the central processor.

4.1 STROBE WAVEFORM

Control is achieved by a reset waveform applied to the second element of the bistable pair and a strobe pulse applied at the input gate of the first element. The strobe is generated by the tape sprocket holes via a delay chain, and a time constant to correspond to the period during which a code signal should be available at the code bistable. Therefore, in the interval between each tape character, the strobe signals at any code bistable input will be at +10 Volts, thus

stopping the information in the buffer from being changed prior to the buffer being reset by the appearance of the next sprocket hole.

In addition, the sprocket pulse also generates reset ($\overline{R/S}$) which is a positive going pulse and is used to reset the Reply statisiser in the A-AQ_3 board. The loading rule requires that further drive should be provided where the number of elements to be driven by one source exceeds four. Thus the Reset pulse is routed through an emitter-follower to the code element at each digit input.

5. CABLE RECEIVERS AND CABLE TRANSMITTERS (A-FX UNIT)

The logic circuits of the A-FX unit implement several functions utilising LSA elements. The logic circuit of the A-FX unit is depicted in Fig. C6.

The overall logic of the Paper Tape Control is depicted in Fig. C2.

5.1 The Logic Circuits of the A-FX Unit

(a) Drive circuits

Eight LSA-01 dual input NAND gates output to eight LSA-11 cable transmitters.

Eight inputs CODE 1 → CODE 8 into the LSA elements with output INPUT READER 1 → INPUT READER 8.

A transmitter loaded with cable and one receiver, switches off for an input of less than 1.2V (logic '1' output) and on for an input of greater than 1.8V

6 +6V AND -6V POWER SUPPLY (A-FY UNIT)

The A-FY Power Unit is essentially a d.c. transformer converting +10, 0, -10V d.c. to +6, 0, -6V d.c. for operation of the

LSA elements on the A-FX unit. The circuit is depicted in Fig. C2.

The two capacitors C1 and C2 decouple the 10V d. c. The base current through R1 to the base of VT1 is stabilised by Zener diode D1, resistor R3 limits current flow through VT1 and adjusts the voltage to +6. 0V d. c. Zener diode D2 and resistor R4 adjust for -6. 0V d. c.

7. PAPER TAPE PUNCH LOGIC

7. 1 (a) Punch Cycle

For a punch instruction the computer generates a Punch Select waveform. If the punch is in a receptive state the Paper Tape Controller will produce a Reply to the Select waveform allowing information from the computer to enter the buffer register.

The incidence of the punch synchronising waveform implements the punch cycle, and after a short delay the pertinent code solenoids, followed by the feed solenoids, are energised, punching out the character and advancing the tape - one character position.

7. 1 (b) Select Reader

The SELECT READER signal is passed through an LSA 12 cable receiver and then an LSA 16 F minilog driver and the output goes to the Select logic on the A-AQ unit.

7. 1 (c) Reply

The output READER REPLY is derived via an LSA -01 NAND gate and an LSA -11 cable transmitter from the REPLY output of the SELECT logic.

7. 1 (d) Punch Select

The SELECT PUNCH signal is passed through an LSA -12 cable receiver and then an LSA 16 F minilog driver and the output goes to the PUNCH SELECT logic on the A-AO unit.

7.1 (e) Punch Reply

The output PUNCH REPLY is derived via an LSA -01 NAND gate and an LSA -11 cable transmitter from the SELECT gate.

7.1 (f) Computer Reset

This waveform is passed through an LSA -12 cable receiver, an LSA-01 NAND gate and is output via an LSA -16 minilog driver to the Tape Out circuitry on the A-AN unit.

7.1 (g) Punch Register Receivers

Eight inputs OP1 → OP8 are received by LSA 17 elements with outputs CODE 1 → CODE 8 which are fed into the Punch Register on A-AM unit.

The receiver is switched off for an input of >2·6V and on with an input of less than 2.0V.

7.2 Synchronisation

The synchronising pulse occurs once per cycle of the motor and from it the punch and feed pulses are derived.

Synchronisation of the tape punch is achieved by means of the synch signal derived by sensing a pulse generated by means of a magnetic insert in the periphery of the punch motor flywheel passing under a pick-up coil.

7.3 Information Waveforms

Information signals to the paper tape punch are in the form of seven information and one parity bit which are derived from drivers connected to the inverse of the accumulator bistables.

A buffer register is inserted between the punch and the computer A Register. Solenoid drivers increase the signal level to the punch solenoids from +6.0V to +28.0V. An eight bit character is punched on receipt of computer instructions 15 6144. If a 5, 6 or 7 track tape is to be used, zeros must be transmitted to the unit in positions corresponding

to the unused tracks.

7.4 Busy Waveforms

Control over the rate at which the Teletype Punch can accept information from the computer is effected by means of a busy waveform which inhibits the reply signal. This waveform is also generated if the tape supply nears exhaustion.

7.5 Re-load

The RE-LOAD control is a manual push button. When operated it extinguishes the Re-Load lamp on the Controller provided that the supply of tape in the machine is not exhausted.

8. TAPE PUNCH CONTROL 2 (A-AO_3 UNIT)

The logic circuit of the A-AO_3 unit is depicted in Fig. C7 and the overall logic in Fig. C2.

8.1 Data Output

A positive going SELECT waveform is applied to the input of a two stage pulser chain which produces a delayed positive going pulse to set the Reply bistable. The output of this bistable is gated with the Select Gate signal to give Punch Reply. The negative going edge of Select is inverted and used to re-set the Reply bistable. A $\overline{\text{SELECT}}$ output is provided for the A-AN unit. The REPLY signal is also sent to the A-AN unit where it is used to generate the setting and re-setting signals for the punch register (A-AM_3 unit) which buffers each character to be punched. Output data designated OP1 to OP8 is routed to the punch register via cable receivers of the A-FX unit.

8.2 Punch Synchronisation

The SYNCH signal from the punch is twice inverted, gated with $\overline{\text{BUSY}}$ and then used to set a bistable which feeds into the RESET circuitry. Simultaneously the SYNCH signal triggers a pulser

whose inverted output is gated with that of the bistable. The resultant waveform is used to trigger a monostable. The monostable gives the output $\overline{\text{MONO}}$ which is used gate data from the punch register to the Solen oid drivers.

The pulser is triggered when $\overline{\text{MONO}}$ goes down to 0V and gives an output λ which is used to reset the bistable. Resetting the bistable triggers a pulser which gives the output waveform RESET. This RESET signal is used to reset the BUSY and RO bistables.

8.3 Run-Out

A run-out signal RO is received from the run-out bistable on the A-AN unit. This signal is fed into a chain of two pulsers which provide a pulse which is then gated with RUN-OUT INHIBIT and BUSY from the A-AN unit. The output of this gate provides the signal RUN-OUT via an inverting element and is also fed into a third pulser which provide a pulse output RUN-OUT BUSY. The RUN-OUT INHIBIT and BUSY signals are gated in to prevent run-out when either SELECT is up or the punch is operating.

9. TAPE PUNCH CONTROL 1 (A-AN$_3$ UNIT)

The functions of A-AN$_3$ unit are complimentary to that of the A-AO$_3$ unit. The logic circuits of the A-AN$_3$ unit is depicted in Fig. C8.

The RESET pulse is timed to coincide with the completion of the punching out of a character and resets the Busy signal to permit subsequent operations to be implemented.

9.1 Reply Inhibit

The logic circuit of the A-AN$_3$ unit enable the Reply signal to be inhibited under certain conditions. At the commencement of a

punch instruction the following waveforms are false, BUSY, MANUAL, RO, RESET, TAPE OUT. This ensures that immediately a Select signal is given, the $\overline{\text{SELECT}}$ goes false resetting the bistable on the A-FN board so that SELECT GATE goes false generating a reply. The Select goes false and when BUSY comes true, the statisiser is set so that any other replies are inhibited. If another Select signal comes true when BUSY is still true, the BUSY signal is prevented from holding the bistable in the inhibit condition and the bistable will be reset by RESET at the end of the cycle. The waveforms RO and MANUAL also set the SELECT GATE false if SELECT is not present. The waveforms TAPE OUT are MANUAL being true prevent RESET from resetting the SELECT GATE The waveforms TAPE OUT, RO, BUSY or MANUAL being true prevent $\overline{\text{SELECT}}$ from resetting the SELECT GATE. The α and β pulsers are generated from the Reply signal α being delayed by β. α is the setting waveform and β the resetting waveform for the punch register on the A-AM unit.

9.2 Computer Reset

The computer reset output of the AF-X unit resets the TAPE OUT bistable, lamp driver L and extinguishes the RELOAD lamp. Computer reset also prevents the punch from operating by holding $\overline{\text{MONO}}$ at 0 Volts.

10. PUNCH BUFFER REGISTER (A-AM_3 UNIT)

The A-AM_3 unit functions as a buffer register between the punch and the computer A Register.

The punch register comprises 8 code bistables, α (setting) and β (re-setting) gates, RUN-OUT decode and the code input gates for information from the Accumulator.

Interposed between the code input gates and the unit lines are eight emitter followers to provide a buffer between the LSA elements of the A-FX unit and the Minilog elements of the A-AM unit.

The logic circuits of the A-AM_3 unit is depicted in Fig, C9.

10.1 '1' Representation

The punch register logic responds to waveforms at the α gates, the input conditions at these points being at 0 Volts where a '1' signal is present.

Inversion at the α gates gives a +10 Volt setting pulse to the second element of the bistable pair in the digit position selected. The resultant output of 0 Volts is strobed by $\overline{\text{MONO}}$ via an inverter and emitter follower, to the Solenoid Driver. When both inputs to the Strobe gate are at 0 volts the element is held in the cut-off condition. This allows a +10 Volt pulse to be applied to the associated Solenoid driver input.

When a '1' is to be represented on tape, the driven solenoid driver energises the operating solenoids at the punch and the hole is punched.

10.2 '0' Representation

In the conditions where a '0' is to be represented, the associated α gate will see an input of 6 Volts from the code input. This condition switches the transistor in the α gate initiating a drop in the output to '0' level, thus preventing the punch register bistable in this digit position from being set.

11. TAPE PUNCH DRIVERS (A-AK_3 UNIT)

The function of the Paper Tape Punch Drivers is to supply drive to the Punch solenoids. The nine punch drivers include

one feed amplifier operating the sprocket hole punch and eight solenoid drivers each operating a punch solenoid in the Paper Tape Punch. The logic circuit is depicted in Fig. C10.

Inputs from the punch register on the A-AM unit are gated with MONO in a minilog NOR circuit and are then applied to the solenoid drivers. The output of these go direct to the feed and punch solenoids.

11.1 Solenoid Operation

In the circuit diagram of the solenoid drive, the two cascaded transistors VT55 and VT 54 normally have a false input and no current flows in the solenoid. When a '1' is to be represented on paper tape, the output from the minilog element to the base of VT55 becomes true. As a result VT54 conducts heavily thus operating the solenoid.

The energised solenoids operate the armatures connected to the perforating pins that punch out character holes in the Paper Tape.

The strobe waveform $\overline{\text{MONO}}$ energises the feed amplifier to punch sprocket holes in the tape at each character position.

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PART 3: PAPER TAPE EQUIPMENT

CHAPTER 4: PAPER TAPE READER MCB 70

CHAPTER 4

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CHAPTER 4

PAPER TAPE READER CAT. NO. MCB 70

1. INTRODUCTION

The MCS 920 Model B Tape reader MCB 70 is an Elliott Photo Electric paper tape reader type T2/218 which operates at a nominal speed of 250 characters per second. It will read five, six, seven and eight track tapes ($\frac{11}{16}$", $\frac{7}{8}$" or 1" wide) of any colour. The tape will stop in less than one sprocket hole pitch under all conditions. (The brake circuits of the paper tape controller are not used in this system).

Details of operation, adjustment and maintenance appear in the Elliott T2/218 Tape Reader Handbook.

2. MECHANICAL CONSTRUCTION

The dimensions of the tape reader are 6" wide, 10" deep and 10" high with a weight of 17 lb. It is a free standing unit with the reading station at the front and the two connections at the rear.

3. SWITCHES

The following control switches are mounted on the reader panel.

(i) ON-OFF. Power Switch

(ii) RUN-OUT. Push button switch runs out tape at full speed

(iii) TAPE OUT. Operates when no tape is present.

4. INTERCONNECTIONS

The Tape Reader is connected to the Paper Tape

Controller by two cables.

SOCKET 3SKT6 to Plug 5PL2 carrying amplified photo cell outputs and amplified power supplies.

SOCKET 3SKT5 to Plug 5PL1. Power supplies for lamp and motor, connections to "tape out", run-out switches and clutch solenoid.

5. POWER SUPPLIES

Power is supplied to the Tape Reader from the Paper Tape Controller. 220-250V, a.c. 50 c/s; + 10V d.c, -10V d.c, 10V a.c.

PAPER TAPE READERS. CAT. NO. MCB 71

1. INTRODUCTION

The MCS 920 Model B Tape Reader MCB 71 is an Elliott Photo electric reader type T5/217 which operates at a nominal speed of 500 characters per second. It will read five, six, seven or eight track tapes ($\frac{11}{16}$", $\frac{7}{8}$" or 1" wide) of any colour.

Details of operation, adjustment and maintenance appear in the Elliott T5/217 Tape Reader Handbook.

2. MECHANICAL CONSTRUCTION

The dimensions of the Tape Reader are $6\frac{5}{16}$" wide $10\frac{1}{4}$" deep and $9\frac{7}{8}$" high and weighing 17 lb. It is a free standing unit with the reading station at the front and with two cable connectors at the rear.

3. SWITCHES

The control switches for operating the unit are as follows:

(i) ON-OFF. Power Switch

(ii) RUN-OUT. Push button switch runs out tape at full speed

(iii) PRESSEL BAR. Operated to load tape into reader and provides adjustment for tape width.

4. INTERCONNECTIONS

The Tape Reader is connected to the Paper Tape Controller by two cables.

SOCKET 3SKT6 to Plug 5PL2 carrying amplified photo cell outputs and amplified power supplies.

SOCKET 3SKT5 to Plug 5PL1. Power supplies for lamp, motor connections to PRESSEL bar and run-out switches and to clutch solenoids.

5. POWER SUPPLIES

Power is applied to the Tape Reader from the Paper Tape Controller. 220-250V a.c. 50 c/s, + 10V d.c, -10V a.c, 10V a.c.

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PART 3: PAPER TAPE EQUIPMENT

CHAPTER 5: PAPER TAPE PUNCH

CHAPTER 5

PAPER TAPE PUNCH MCB 74

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CHAPTER 5

PAPER TAPE PUNCH MCB 74

1. INTRODUCTION

The Westrex tape punch is equipped with a Teletype BRPE reperforator operating at a nominal speed of 110 characters per second. Operation is in a synchronous mode, one character being punched if available at each revolution of the mainshaft of the unit. A synchronizing pulse generated by a magnetic device on the mainshaft gates the logic circuits to operate the punch and feed solenoids.

Details of operation, adjustment and maintenance appear in the Teletype B. R. P. E. Technical Manual.

NOTE: This punch is for use with Paper Tape Controller (MCB 60) only.

2. MECHANICAL CONSTRUCTION

The dimensions of the unit are $9\frac{1}{2}''$ wide, $16\frac{1}{2}''$ deep and 14" high with a weight of 48 lb. The socket for power and control are at the rear of the unit. The punching station is at the front.

3. SWITCH CONTROLS

Controls on the punch include the following:-

(i) ON/OFF. Power Switch

(ii) Tape width adjustment turret

(iii) RUN-OUT lever

(iv) Low tape detector

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PART 3: PAPER TAPE EQUIPMENT

CHAPTER 6: PROGRAM LOADING UNIT

CHAPTER 6

PROGRAM LOADING UNIT

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LIST OF FIGURES

CHAPTER 6

PROGRAM LOADING UNIT

1. INTRODUCTION

The Program Loading Unit is designed to load the Computer with programs from eight track paper tape punched in the ASC11/4100/903 format. The unit reads paper tape at 20 rows per second loading, 1,000 words in approximately $2\frac{1}{2}$ minutes. The logic of the Program Loading Unit is given in Fig. C11.

2. CONSTRUCTION

The Program Loading Unit is fitted into a standard 17" long x 10" high x 9" deep ribbed aluminium alloy sheet metal equipment cabinet modified with notched hinged brackets for 19" rack mounting (Fig. b refers).

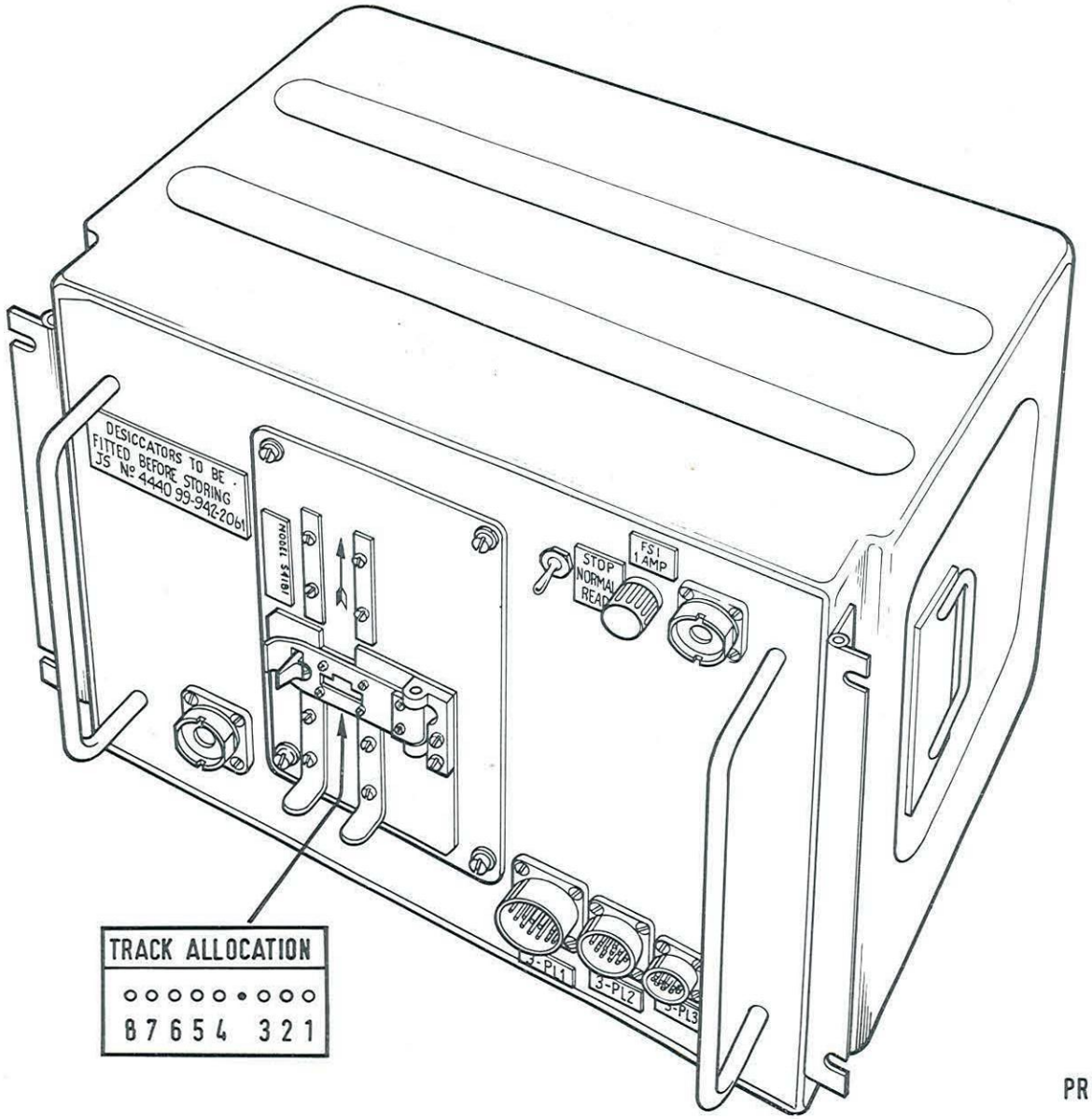
The unit may be sealed for storage by fitting the cover and a pressure relief valve fitted for air transportation. The assembly of the unit is given in Fig. C12, Sht 1 and Sht 2.

The mechanism of a Creed tape reader is affixed to the front panel of the unit by four screws. Additional information on the Creed tape type S4181 reader may be obtained from the manufacturer.

The operating switch, fuse holder, three sockets for cables and two carrying handles are mounted on the front panel of the unit. A cover equipped with captive screws is provided to fit over the front panel of the unit.

Two additional carrying handles fold into recesses at both sides of the unit.

The components within the interior of the unit comprise a power supply switched by a relay with two standard size logic boards and a fixed tagboard with solenoid drive circuitry.



PROGRAM LOADING UNIT
(CAT. No. M.C.B.62)

Fig. b.

3. INTERCONNECTIONS

The interconnections of the 920B Computer System including the Program Loading Unit are given in Fig. A1 (Pt. 1, Chap. 1, Sec. 1).

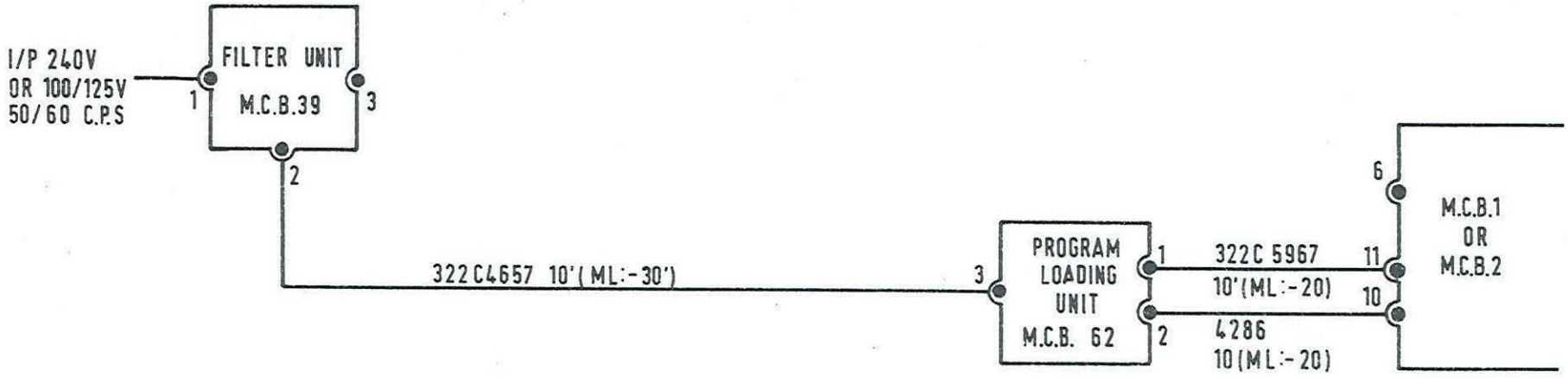
Interconnections between the Program Loading Unit, Filter Unit, Computer Power Supplies and Control Unit are given in Fig. c.

Connections to the unit are by means of connectors 3-PL1, 3-PL2 and 3-PL3 giving the following interconnections.

3.1. Without a Control Unit

3.1.1 Connections from Program Loading Unit to Computer are by 3-PL1 to computer connection 1-SKT 11 and 3-PL2 to computer 1-SKT 10.

When the Program Loading Unit is connected to 1-SKT 11 (Fig. C13 refers) the circuit arrangement of the connection at 3-PL1 allows the program to be started at the Start Address 8181 of the Initial Instructions. This circuit configuration is similar to that of the Start Address Plug (which simulates the address 8177 (Fig. C14 refers). The only difference between the addresses 8177 and 8181 is bit 3 which for 8181 must be at logic '1' at the M-Register. This is achieved by connecting pin D($\overline{\text{NG3}}$) of 1-SKT 11 to pin Z in 3-PL1 of the Program Loading Unit. From Fig. C13 it can be seen that this point is taken to 0 volts by the link connection D to Z of 3-PL1 and from Z of 1-SKT 11 to Z of 3-PL2. Thus a logic '0' applied to the A-FS receivers unit in the Computer is inverted to place a logic '1' in bit position 3 of the M-Register (A-FA).



Central processor with program loading unit.

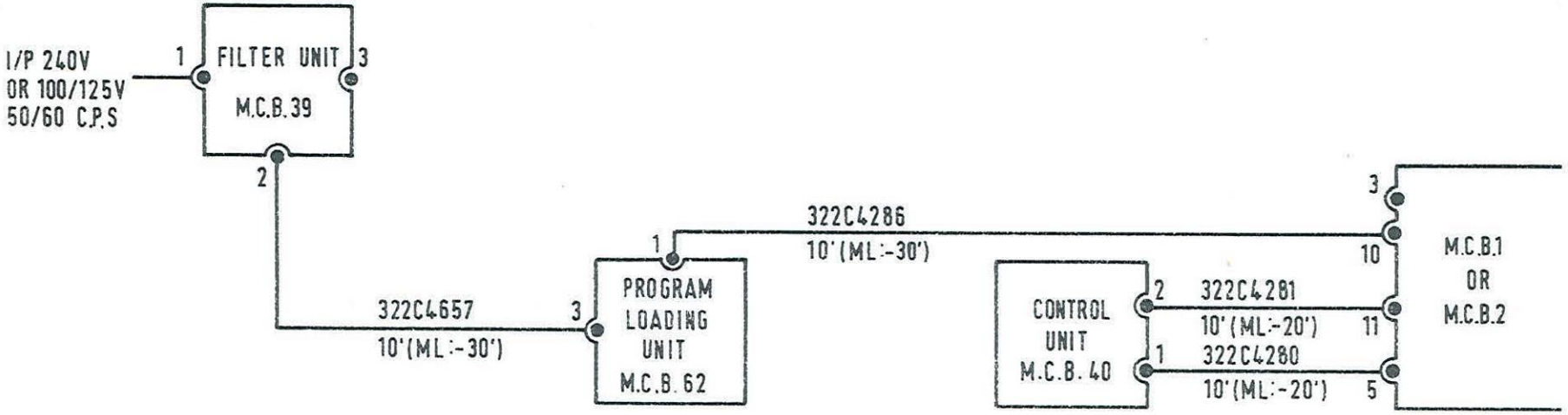


Fig.c Central processor with Program Loading Unit and Control Unit. (Issue 1)

The remaining 12 address bits at 1-SKT 11 on Fig. C13 are open circuit, they are defined as logic '1' and set the M-Register. To complete the binary number corresponding to 8181 however logic '0' must appear at bits 2, 4, 4, 15, 16 and 18 at the M-Register. This is achieved by inserting A-FS receivers to convert these bits from logic '1' to logic '0'. Logic details may be seen in Fig. A13 (Pt. 1, Chap. 4).

3. 1. 2 Connections from the Program Loading Unit to Mains filter are from 3-PL3 to filter 9-SKT 2.

3. 2. With a Control Unit

3. 2. 1. Connections between Program Loading Unit to Computer are from 3-PL1 to computer 1-SKT 10.

3. 2. 2 Connections between Program Loading Unit to Mains Filter Unit are from 3-PL3 to filter 9-SKT 2.

3. 2. 3 3-PL2 is not used.

3. 2. 4 Connections between Control Unit and Computer are from 2-PL1 to computer 1-SKT 5 and from 2-PL1 to 1-SKT 11.

3. 3 Interconnections between 3-PL1 Program Loading Unit and 1-SKT 11 of computer.

TABLE 1

3-PL1	CONNECTIONS	1-SKT 11	FUNCTION
A	Mains Earth	A	Mains Earth
D	Link to Z	D	$\overline{\text{NG3k}}$
W	Link to X, Y, f, h and e	W	INT1k
X	Link to W, Y, f, h and e	X	INT2k Linked to 0V
Y	Link to W, X, f, h and e	Y	INT3k
Z	Link to D	Z	Auto start link to 1-SKT 10
e	Link to W, X, Y, f and h	e	Computer 0 volts
f	Link to W, X, Y, f, h and e	f	ONG k Linked to 0V
h	Link to W, X, Y, f, h and e	h	ENG k
j	RESET	j	RESET k
r	Link to s	r	Auto start link to Computer for MCB 21 Power Unit
s	Link to r	s	0 volts

3.4 Interconnections between 3-PL2 Program Loading Unit and 1-SKT 10 of Computer.

TABLE 2

3-PL2	1-SKT 10	FUNCTION
A	A	IR1
B	B	IR2
C	C	IR3
D	D	IR4
E	E	IR5
F	F	IR6
G	G	IR7
H	H	IR8
T	T	Mains Earth
V	V	READER SELECT STR
W	W	READER REPLY RTR
Z	Z	Auto start link to Z1-SKT 11
d	d	COMPUTER RESET
e	e	COMPUTER 0V
f	f	Relay Supply 24V (+ VE)
g	g	Relay Supply 24V (- VE)

3.5 Interconnections between 3-PL3 Program Loading Unit and 9-SKT2 Mains Filter.

TABLE 3

3-PL3	9-SKT2	FUNCTION
A	A	Line
B	B	Neutral
C	C	Mains Earth

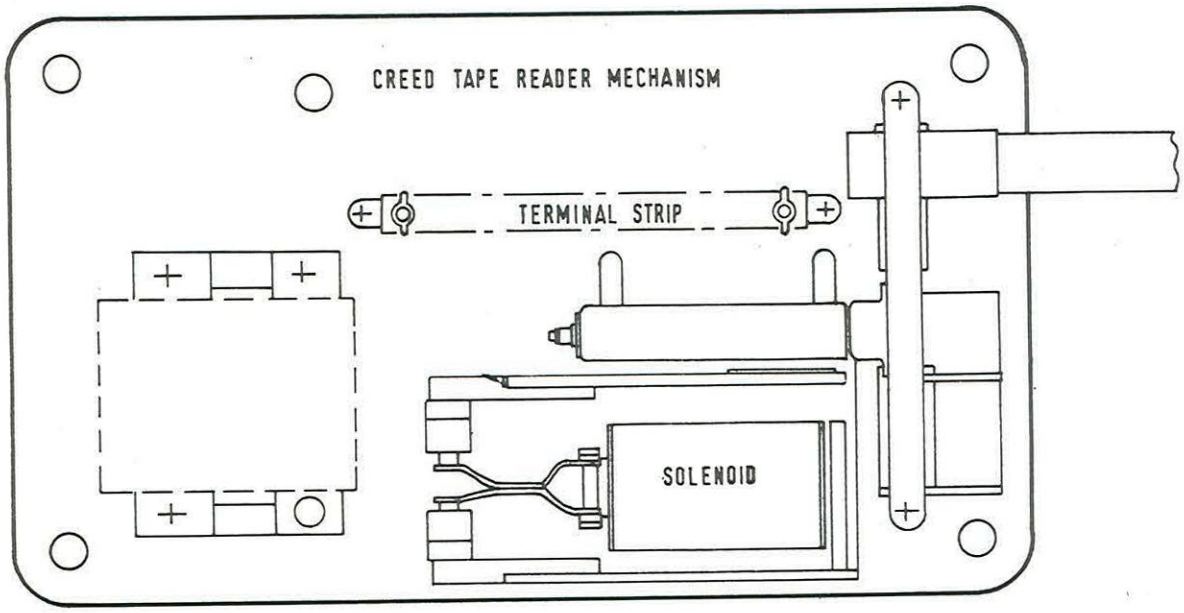
3.6 Connections to the Creed S4, 181 Tape Reader

The signal path from the Creed Tape Reader mechanism to the Buffer Register on the 4/A-LA unit is by means of a short multi-wire captive cable terminating in a 33 contact Jones plug mating with SKT 6 in the interior of the unit (Fig. C12 refers). Mark space and tongue contacts are each brought out separately to terminals 1 to 24 for each of the 8 channels. Tape Out contacts are 26 and 27. Tape Feed are 29 and 30. The operating power to the mechanism solenoid is applied to pins at 31 and 32. The Jones plug, wiring and some component layout of the Creed Reader are depicted in Fig. d.

4. POWER SUPPLY

A schematic diagram of the Power Supply is given in Fig. C11.

The mains input to the Program Loading Unit utilises an electrostatically screened isolating transformer for noise reduction with the following tappings ± 10%, 250, 240, 230, 220, 210, 200, 125, 120, 115, 110, 105 and 100 volts at 50 c/s. The Power Supply provides the following voltages.



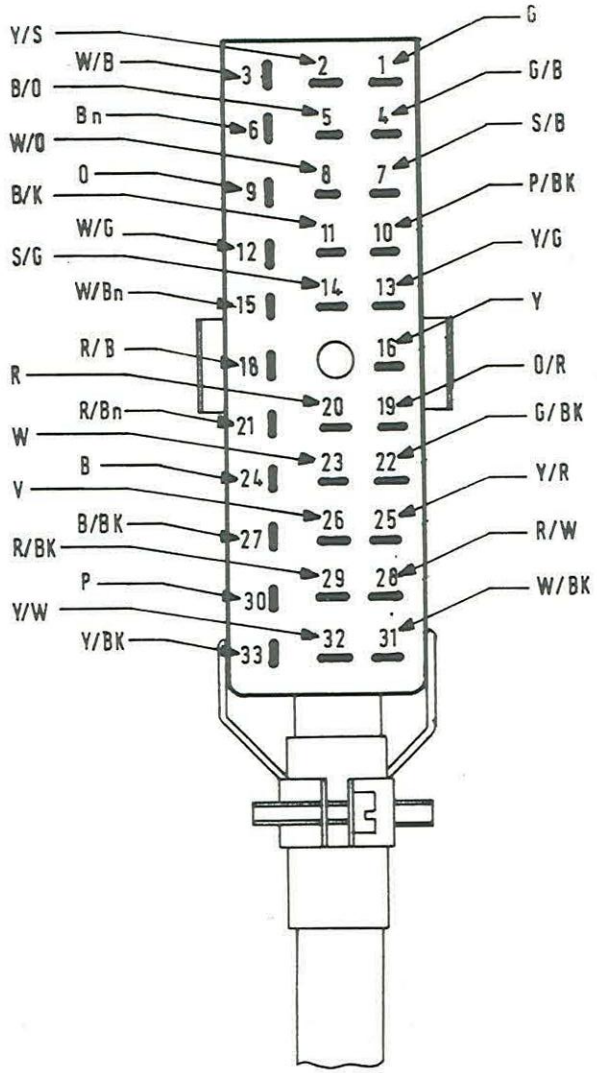


Fig. d Creed tape reader Mechanism and Jones plug connector

Issue 1

(i) + 24V (+ VE) d. c.

(ii) + 24V (- VE) d. c.

(iii) + 6. 5V d. c.

(iv) - 6. 2V d. c.

(v) 0 volts

5. SWITCH CONTROL

The three position switch S1A, S1B located on the front panel of the unit operates in positions READ, NORMAL and STOP.

5. 1 READ (Non-locking position)

If the tape reader has been loaded with tape, operating the switch momentarily from NORMAL to READ and returning to NORMAL again will implement a READ operation. If the Program Loading Unit is connected in place of the Control Unit and the computer switched on, the computer is RESET and then jumps into location 8181, the entry into Initial Instructions. The Automode connections with the Program Loading Unit are given in Fig. C13.

5. 2 NORMAL

Switch S1 normally remains in the NORMAL position which is open circuit. No action can thus be implemented unless the switch is first operated to READ or to STOP. When operated to READ and released it returns to NORMAL.

5. 3 STOP (Locking)

Operating switch S1 to the locking STOP position will immediately stop the Tape Reader. However if the machine has been previously operating the READ operation will automatically be resumed if the switch is returned to the NORMAL position.

6. START ADDRESS PLUG

The Start Address Plug is used when it is desired to use a program within the store instead of reloading a program (Fig. C14 refers). In this instance the Program Loading Unit is disconnected from the computer and a Start Address Plug connected in its place. When the computer is switched on, it will jump to location 8177 . The Program Loading Unit need only be connected to reload a program.

7. OPERATION OF THE PROGRAM LOADING AND CONTROL UNITS

The Program Loading Unit is switched on and off at the same time as the computer power supplies by means of a 24V control line from the computer power supply.

8. POWER SUPPLY CIRCUITS

All power supply voltages of the Program Loading Unit are isolated from the chassis as shown in Fig. C11.

When the power is switched on relay RL1 is activated closing contacts RL1/6 and RL1/3 connecting mains power from filter unit 9-SKT2 to the primary of transformer T1.

The three secondary windings supply 29V a. c., 12V a. c. and 8V a. c. to their respective rectifying circuits.

8. 1 + 24V (+VE), + 24V (- VE) d. c.

Diodes D12 and D13 rectify 29V a. c. in a single phase full wave rectifier circuit to give + 24V (+VE) and + 24V (- VE). The output is smoothed and filtered by the R.C. combination R13, R14, C6, C7 and C8. The d. c. output is stabilised by the series regulator VT5 controlled by a reference voltage at the cathode of Zener Diode D7 developed across R15, R16, D7 and D8. The stabilised output appears across R17 and R18.

8.2. + 6.5V d.c., 0 volts

This voltage is generated by the full wave rectification of the 12V a.c. output of T1. The rectified output of D4 and D14 is filtered by the R.C. combination R19, C9. Shunt stabilisation is achieved with Zener Diode D9. R20 limits current flow.

8.3 - 6.2V d.c.

The a.c. source of this negative supply is the 8V a.c. output of T1. The rectified output at Diodes D5 and D6 are connected to 0V of the 6.5V d.c. supply. Capacitance filtering is effected by C5. Zener Diode D10 affords shunt regulation with R12 limiting current flow.

9. CONTROL LOGIC CIRCUITS

The logic units controlling the Read operation are:

(i) 5/A-LB Unit Control Logic

(ii) The T-R Board. Drive Unit

(iii) The 4/A-LA Unit. The Buffer Register

The A-LB unit controls the T-R Board which drives the solenoid mechanism of the Tape Reader.

The A-LA unit functions as an 8-bit Buffer Register between the Tape Reader and the central processor and also controls the tape feed.

9.1 Reader Operation Sequence

9.1.1 Normal Cycle

During operation the timing of the sequence is determined by the pulse generators and delay units in the 5/A-LB unit.

9.1.2 Start Cycle

If the tape reader has been loaded with tape and the switch S1 operated to Read, a tape input instruction from the computer generates a READER SELECT waveform which as READER REPLY signals the computer if a character is available on the Input Reader (IR) lines.

The Reply signal permits the computer to receive information from the Input Reader lines and cancels SELECT. Reply will only be sent if the unit has been loaded with tape and S1 operated. This information is the output of the tape reader mechanism. The back edge of the SELECT waveform energises the electromagnet drive logic operating the Creed Tape Reader mechanism. The pins of the sprocket wheel engage corresponding holes in the tape which is advanced one character for each pulse operating the electromagnet. When the electromagnet is de-energised at the end of the feed pulse, the tips of spring loaded peckers rise to sense the code combination and load the buffer. The peckers which enter the holes in the tape connect the Mark contact to Line. A tongue associated with the pecker held down by unpunched tape connects the Space contact to Line. As the next pulse advances the tape to bring a new character to the sensing point, a bail arm depresses the peckers so that they are held clear of the tape until the tape feed action is terminated.

9.2 Reader Control Logic

The overall logic of the Program Loading Unit is depicted in Fig. C11. The conditional waveforms input to the Control logic, set and reset bistables (and/or switch elements) are as determined by voltages at the control switch of the Program Loading Unit and by computer demand.

9. 2. 1 Reader Operating Conditions

When the Program Loading Unit is operating, the reader will accept a reply provided:

(1) Tape is in the reader

(2) The reader has been loaded by depressing the switch to the Read position

(3) The Busy statisiser M/01-L/02 is not set

9. 2. 2 REPLY

Refer to Fig. C11 and for waveforms to Fig. f.

When a character is to read by the computer from the loaded buffer, the READER SELECT waveform goes to a logic 'one'. The output of L/02-13 falls to a logic 'zero' so that the READER REPLY line goes to a logic 'one' provided that:

(1) The solenoid drive bistable (M/01-L/02) is not set

(2) When pins 5 and 6 at L/02-13 will be at logic 'zero'

9. 3 Drive Unit (T-R TAG BOARD)

The components of the T-R board are assembled on a printed circuit board and affixed to its mounting position by four screws. The lay-out and assembly of the T-R board is given in Fig. e.

9. 3. 1 The Circuit of the T-R Board

The function of the T-R Board is to amplify a pulse from the Control Logic to drive the electromagnet of the Creed Tape Reader.

The circuit of the T-R Board is given in Fig. C11 and comprises four transistors, three diodes and associated capacitors and resistors.

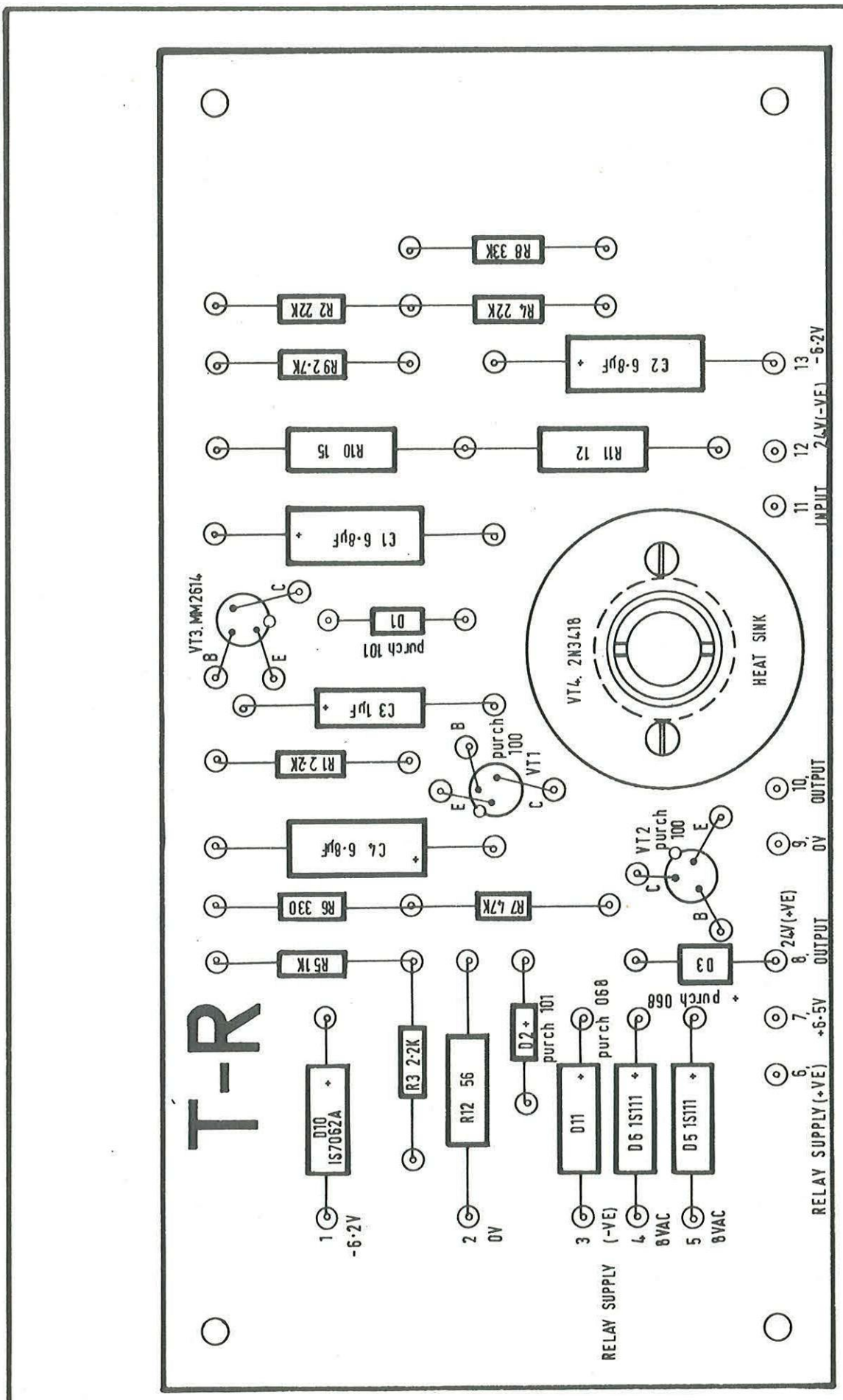


Fig e. T-R board layout and assembly, Component side view. Issue 1

When the input to Diode D1 becomes a logic 'zero', VT1 is switched off. This turns on VT2 which switches off VT3. The output of VT3 turns on VT4 which operates the tape reader solenoid.

The + 24V (+VE) and + 24V (- VE) connections to the T-R Board are by screened cable.

The remaining voltage inputs are + 6.5V, -6.2V and 0 volts.

9.4 Buffer Register (4/A-LA Unit)

The components of the A-LA unit are mounted on a printed circuit plug-in board. An example of this may be seen in Fig. A2 (Pt. 1, Chap. 1); and pertinent waveforms in Fig. f.

9.4.1 The Circuit of the A-LA Unit

One section of the A-LA Unit functions as an 8-digit buffer register accepting the Mark and Space output of the tape reader. When loaded, the contents of this buffer are gated into the computer by REPLY going true.

The A-LA buffer register comprises eight statisiser elements with a transmitter at the output of each statisiser. The eight outputs are IR1 ——► IR8. Input connections to these statisisers from the tape reader are made so that Mark signals (CODE 1 ——► CODE 8) appear as logic 'one' and Space signals (CODE 1 ——► CODE 8) appear as logic 'zero' at the transmitter output.

9.4.2 The Tape Feed Statisiser

The Tape Feed statisiser functions to prevent a second character being read if the mechanism has failed to advance the tape. This is achieved by the waveform K/01-13 initiating a solenoid drive pulse, and also setting the Tape Feed statisiser. In this state it prevents the Busy statisiser being reset at the end of a cycle. However if the tape has moved correctly

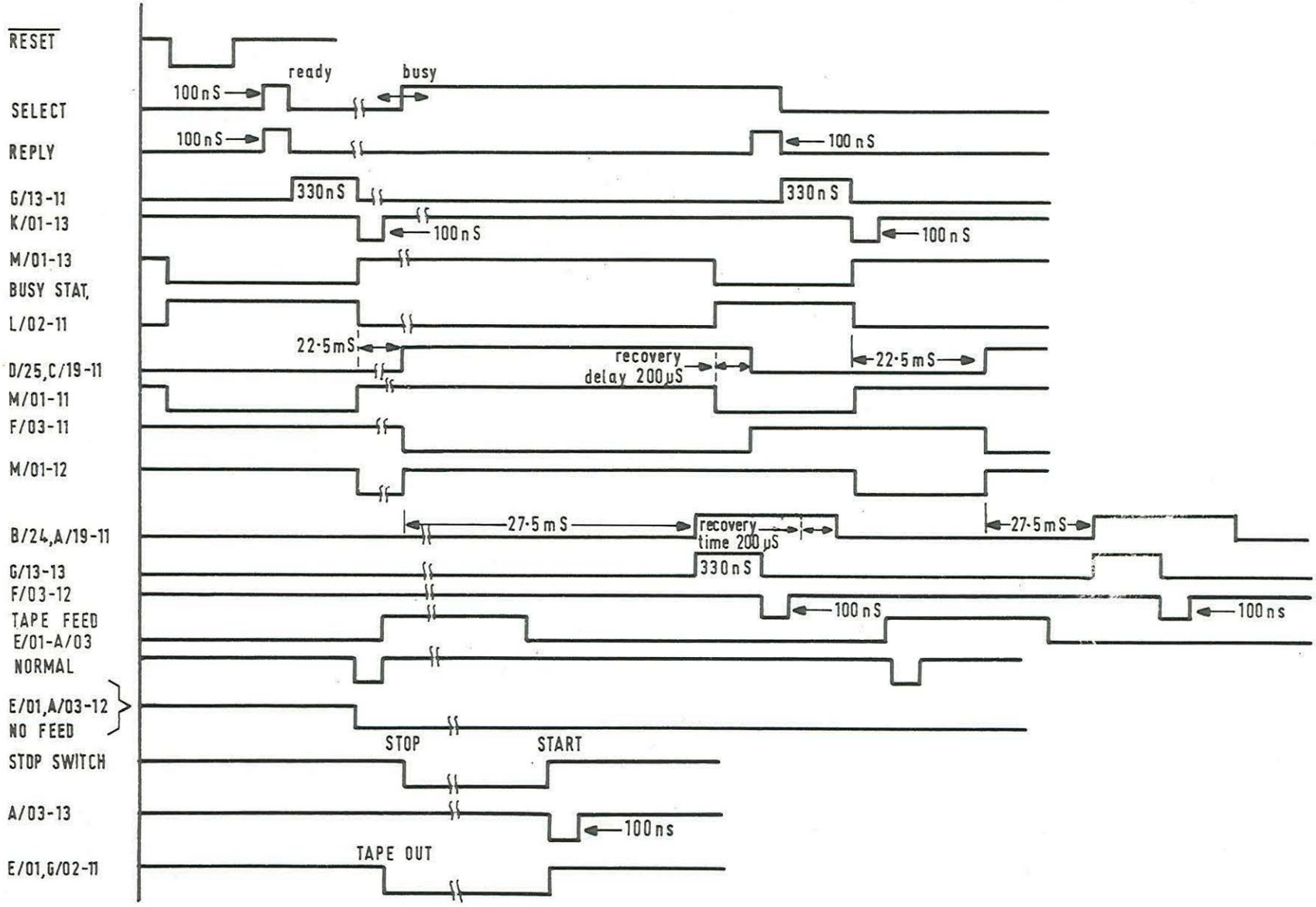


FIG. f Program Loading Unit Waveforms Note: Not to scale. Issue 1.

the Tape Feed contacts will change over and reset the Tape Feed statisiser. This action allows the next character to be read by resetting the Busy statisiser.

The Tape Feed statisiser can be reset manually by switch S1A.

9.4.3 The Tape Out Statisiser

The Tape Out statisiser E/01-G/02 is set when the Tape Out contacts are made. When in this state it prevents another character being read by inhibiting the resetting of the Busy statisiser at the end of the cycle. To resume the reading operation, the tape reader must be reloaded with tape and the Tape Out statisiser reset by operating switch S1A to Read.

9.5 Control Logic (5/A-LB Unit)

The 5/A-LB unit is similar in construction to the 4/A-LB unit (see Section 9.4).

9.5.1 The Circuit of the A-LB Unit

The A-LB unit contains the basic timing loop of the solenoid drive circuit. The back edge of the Reply waveform is used to initiate a pulse at K/01-13 which sets the Busy bistable M/01-L/02. See Fig. f.

The output L/02-11 is fed into a 22.5 msec. delay unit D/25-L/19, the delayed output is incremented by F/03-11 and gated by M/01-11 to implement a 22.5 msec. solenoid drive pulse M/01-12.

The 27.5 msec. delay unit B/24-A/19 is inhibited in the timing loop to give the machine time to recover after a solenoid drive pulse. At the end of the 27.5 msec. delay, a pulse is sent via F/03-12, H/01-12 and H/01-13 to reset the Busy statisiser thus allowing the next character to be read.

MCS 920B COMPUTER TECHNICAL MANUAL

CATALOGUE NO. MCB 143

PART 3: PAPER TAPE SYSTEM

CHAPTER 7: PAPER TAPE STATION MCB 66

CHAPTER 7

CONTENTS

LIST OF FIGURES

CHAPTER 7

1. PAPER TAPE STATION

1.1 Introduction

The MCB 66 Paper Tape Station comprises a number of discrete units which may be arranged as desired. Connections to the 920B Computer are given in Fig. A1 (Pt. 1, Chap. 1).

1.1.1 Component Units

The component units include the following:

Power Supply

Paper Tape Control Logic

Paper Tape and Teleprinter Controller MCB 66

Paper Tape Punch MCB 66C

Paper Tape Reader MCB 66B

Mains Filter MCB 39

A typical assembly of these units is given in Fig. C15.

1.1.2 Logic Boards

The circuits of the L. S. A. elements used on the logic boards are described in Part 1, Chapter 2 of this Manual. The tables in Fig. C24 provide details of the types of L. S. A. elements on each board and the location of any extra components used.

On the logic diagrams, signals to and from the central processor are enclosed in square brackets [ ] and signals to and from the teleprinter are enclosed in diamond brackets < >. All discrete components, not being part of the sub-assemblies are fitted in Area G of the logic board, Fig. g refers.

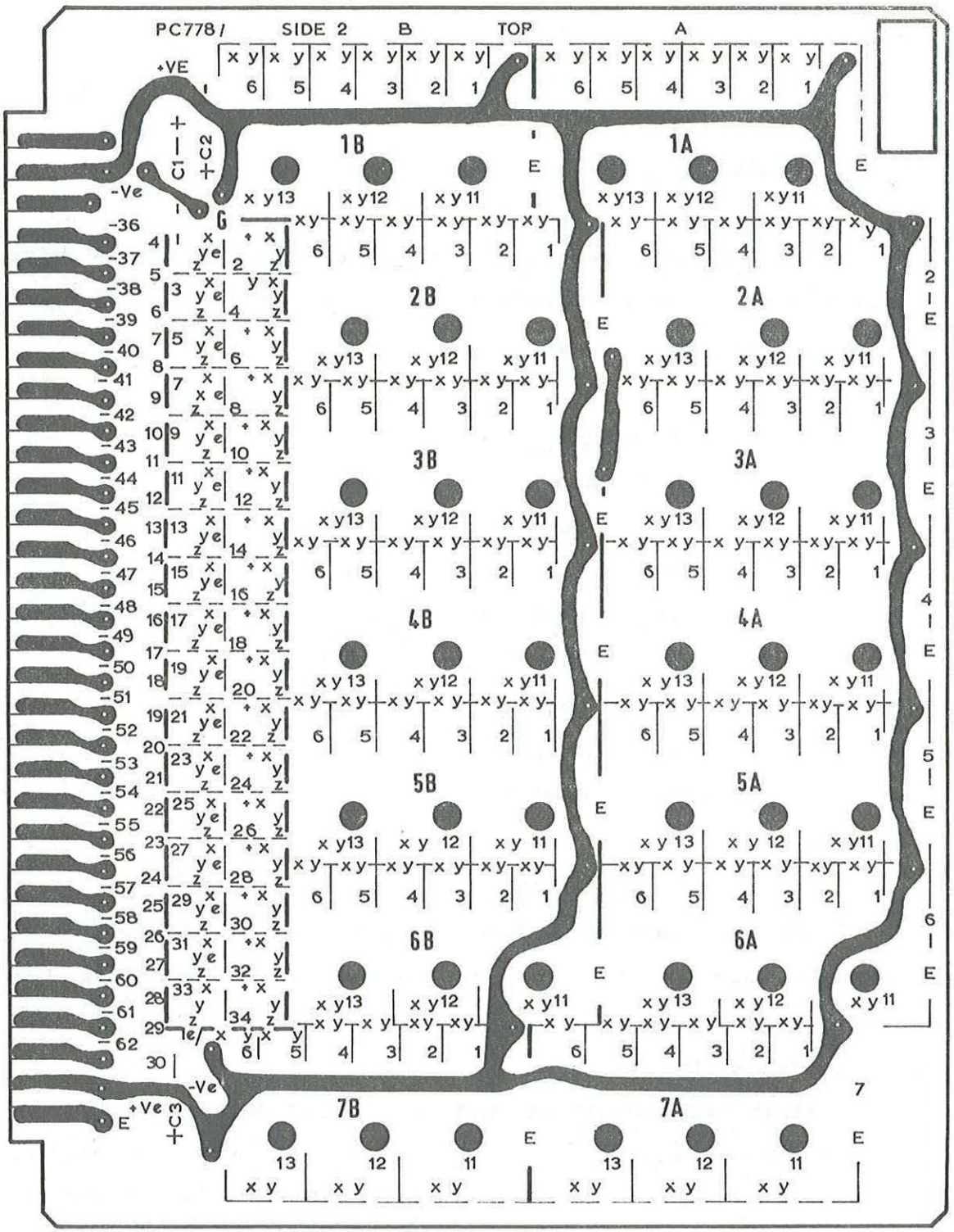


Fig. g. Typical Logic Board showing G area (MCB66) Issue 1

1. 2 Interconnections

The interconnections within the Paper Tape Station, the mains input from the filter unit and the computer interface, are given in Fig. C16

1. 2. 1 Interconnections between the Computer Interface and Paper Tape Logic

COMPUTER INTERFACE TO PAPER TAPE LOGIC

1-SKT 10	TO 18-CNA	FUNCTION
A	4	IR1
B	12	IR2
C	18	IR3
D	25	IR4
E	31	IR5
F	37	IR6
G	43	IR7
H	49	IR8
J	8	OP1
K	15	OP2.
L	22	OP3
M	28	OP4
N	34	OP5
P	40	OP6
R	46	OP7
S	52	OP8
T	11	Earth
U	20	Address Bit 3
V	51	STR

COMPUTER INTERFACE TO PAPER TAPE LOGIC (Cont'd)

1-SKT 10	TO 18-CNA	FUNCTION
W	57	RTR
d	38	RESET
f	44	+24V
g	50	+24V
h	64	STP

1. 2. 2 Interconnections between Control Station Power Supply and Pape Tape Logic

CONTROL STATION POWER SUPPLY TO PAPER TAPE LOGIC

19-CNA TO 18-CNE	FUNCTION
A	OUT 1
B	OUT 2
C	OUT 3
D	OUT 4
E	OUT 5
F	OUT 6
H	OUT 7
J	OUT 8
K	OUT 9
L	Feed
N	Tape Low
R	Link

CONTROL STATION POWER SUPPLY TO PAPER TAPE LOGIC (Cont'd)

19-CNA TO 18-CNE	FUNCTION
S	Sync
T	-VE
a	Clutch
d	Screen
e	Tape Out
f	Run Out
h	0V
p	-6V
m	+6V
n	+6V
r	0V
s	+6V
v	0V
w	+28V
y	0V
z	0V
AA	+28V
CC	0V
EE	+28V
HH	0V

1. 2. 3 Interconnections between Control Panel and Paper Tape Logic

CONTROL PANEL TO PAPER TAPE LOGIC

17 SKT 1 TO 18-CNB	FUNCTION
R	+28V
F	0V
A	Reload (Lamp)
D	Reload
J	Run Out
C	Out Punch
H	Out Auto
E	Demand
M	In Auto
S	In Reader
K	Hold Up
P	Stop (Lamp)
N	Stop
U	Read (Lamp)
T	Read
B(18-CNB)a	Tape Low linked to L
L(18-CNB)b	Linked to B

1.2.4 Interconnections between Control Station Power Supply Unit and Mains Filter

POWER SUPPLY TO MAINS FILTER

19-TB1 TO 9-SKT 2		FUNCTION
10	A	Line
11	B	Neutral
12	C	Earth

1.2.5 Interconnections between Control Station Power Supply and Paper Tape Punch

POWER SUPPLY UNIT TO PUNCH

19-CNC TO 4-SKT 1		FUNCTION
A	8	OUT 1
B	1	OUT 2
C	2	OUT 3
D	3	OUT 4
E	4	OUT 5
F	5	OUT 6
H	6	OUT 7
J	7	OUT 8
K	9	FEED
L	16	+28V
M	17	+28V

POWER SUPPLY UNIT TO PUNCH (Cont'd)

19-CNC TO 4-SKT 1		FUNCTION
N	18	+28V
S	12	Sync
T	24	-VE
V	-	Screen
	11	Screen
b	12	Tape Low
19-TB1 TO 4-SKT 2		
1	Copper Screw	Line
2	Brass Screw	Neutral
3	Screen	Earth

1.2.6 Interconnections between Control Station Power Supply Unit and Paper Tape Reader

POWER SUPPLY UNIT TO READER

19-CNB TO 5-SKT 1		FUNCTION
A	A	Clutch
B	B	+28V Clutch
C	C	-
D	O	-
E	D	Linked to E and N
N	P	-

POWER SUPPLY UNIT TO READER (Cont'd)

19-CNB TO 5-SKT 1		FUNCTION
	E	Linked to D and N
	N	Linked to D and E
19-TB1 TO 5-SKT 1		
4	Q	Line
5	R	Neutral
6		Earth Screen

1. 2. 7 Interconnections between Logic and Reader

LOGIC RACK TO READER

18-CNC TO 5-SKT 2	FUNCTION
A	R1
B	R2
C	R3
D	SPKT
E	R4
F	R5
P/G	R6
H	R7
J	R8

1.3 Power Distribution

1.3.1 A.C. Supplies

The distribution of the a.c. supplies is given in Fig. C17.

The mains input on TB1/10, 11, 12 is taken to the contacts of RLA. This relay is energised by a 24V signal from the interface which is present when the mains ON button on the Computer Control Unit is operated. A Local/Remote switch is available to by-pass the relay contacts when it is required to apply power to the Paper Tape Station only.

The mains supply to the punch motor is switched by a silicon controlled rectifier (SCR) which is energised by a signal from the punch logic.

The 9.5V a.c. output of the Transformer CVT is used to light the lamp in the tape reader.

1.3.2 D.C. Supplies

The distribution of the d.c. supplies is shown in Fig. C18.

The d.c. supplies are provided by two units labelled PSA and PSB. PSA is a type NS-ELL/006 and provides the +6V and -6V supplies at current ratings of 3A and 1A respectively. PSB is a type ES 1000/28, and provides the +28V supply at a current rating of 10A.

Details of these units can be obtained from the manufacturer's handbooks.

1.3.3 Over-Voltage Protection

An over-voltage protection circuit is connected across the +6V and -6V d.c. outputs to protect the logic boards from damage due to a rise in level of either of these supplies. Under normal operating conditions, the lamps will be lit and no current taken by the circuit.

If either of the d. c. outputs start to rise, current will be drawn through the corresponding Zener diode and applied to the thyristor. Dependent on the ambient temperature and component tolerances, the thyristor will be triggered when the d. c. level has risen to a value between 6. 5V and 10. 0V.

When the thyristor conducts, a short circuit is applied across the output terminals of the power unit, blowing the appropriate fuse and extinguishing the lamp.

1. 4 Paper Tape Input Logic

1. 4. 1 Introduction

This section contains a functional description of the logic associated with the paper tape. The logic is shown in Figs. C20 and C21.

1. 4. 2 Typical Cycle

Assuming the reader has been loaded, a brief description of the normal cycle of events is as follows:

On receipt of an input select signal, a timing sequence is initiated which gates the data from a buffer register onto the interface lines and then sends a reply to the central processor.

The data is accepted by the processor and the input select signal removed. This causes the reader clutch solenoid to be energised and the tape advanced. When a sprocket hole is detected, a loading timing sequence is started which resets the buffer register and gates the data from the new character into the register. The clutch solenoid is de-energised and the tape movement stopped.

The reader stays in this position until another input select signal is received from the central processor.

1.4.3 Channel Selection

An input from the tape reader is selected according to the position of the Select Input switch and/or the type of system in use. (This is accomplished by operating the necessary controls on the Teleprinter and Paper Tape Controller. Fig. C19 and Fig. h refers. For an input to be taken from the reader RIN must be true.

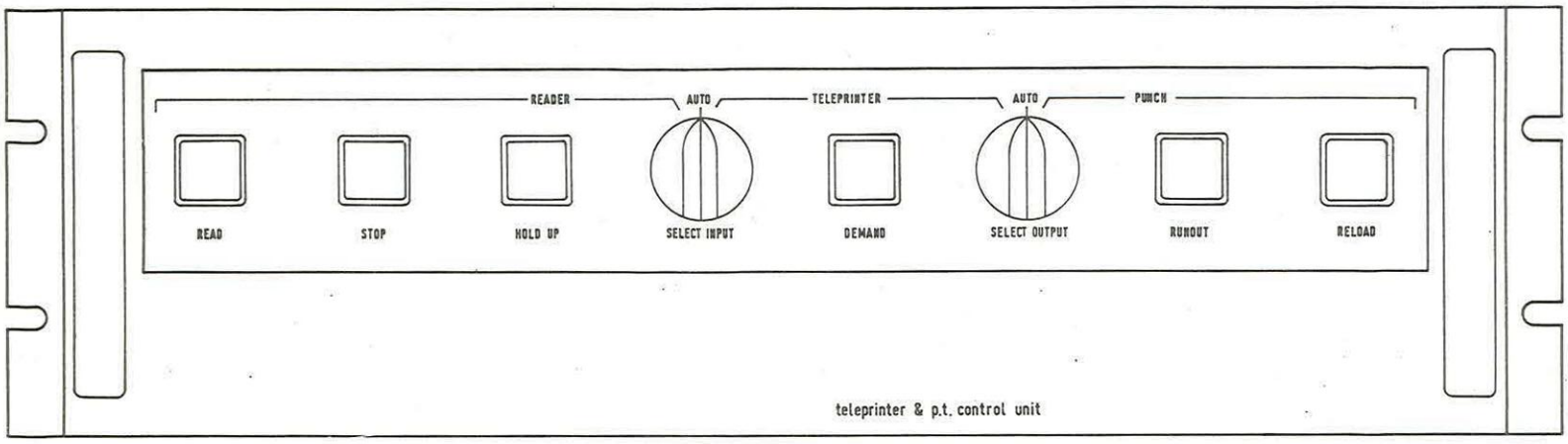
If a teleprinter is not used its associated logic is omitted, and the T/P LINK on board 22 will not be present. This holds the input to gate 14/2B (i.e. board 14, element 2B) at a true level and means that TIN is always false and RIN always true. The position of the Select Input switch has no effect on the logic.

When a teleprinter is used, TIN will be false and RIN true if the Select Input switch is set to READER, or AUTO with the interface signal [ADDRESS BIT 3]false. TIN will be true and RIN false if the Select Input switch is set to TELEPRINTER, or AUTO with the interface signal [ADDRESS BIT 3]true.

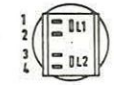
1.4.4 Data Flow

Data from the reader in the form of an 8-bit character $\langle \overline{R1} \rangle$ to $\langle \overline{R8} \rangle$ is stored in a buffer register 1A/1A etc., on board 7, until demanded by the central processor. The buffer is reset by R/S going true and is immediately loaded due to GATE going true.

When a data transfer is required, the signal RDIN is made true and the contents of the buffer gated, at 1A, 2A, etc., on board 15, to the interface input lines [IR1]to[IR8]. The data remains on the lines until accepted by the processor, when RDIN will go false.

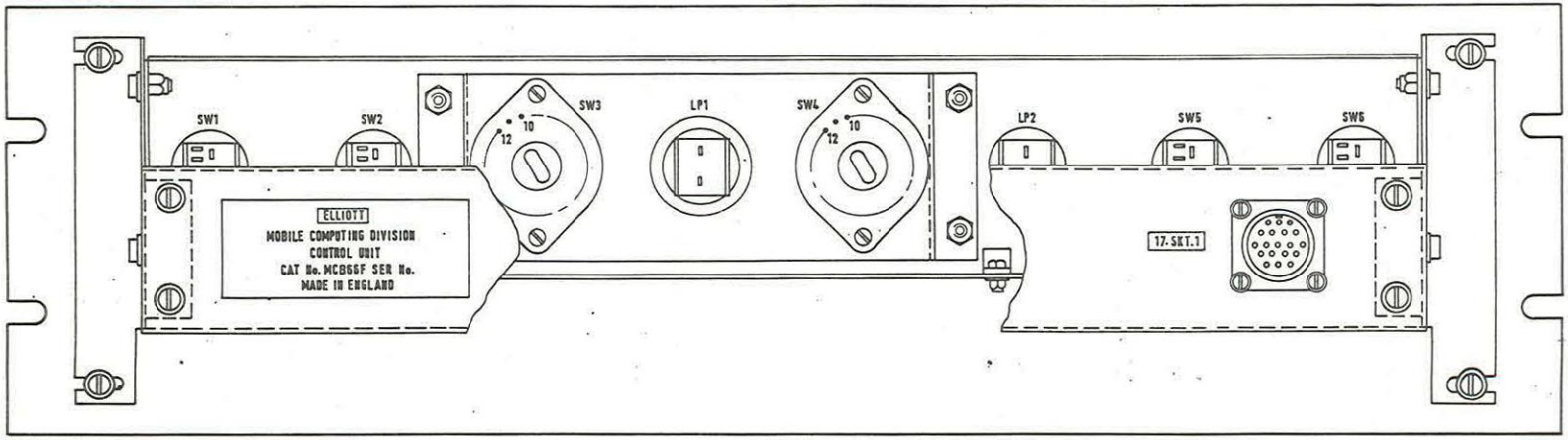


FRONT



PIN IDENTIFICATION FOR SW1, SW2, SW5 & SW6

PIN IDENTIFICATION FOR LP1 & LP2



REAR

Fig. h.

PAPER TAPE STATION MCB66
TELEPRINTER & P.T. CONTROLLER

Issue 1

1.4.5 Reader Timing

1.4.5.1 Data Transfer

When a data transfer is required, interface signal [STR] is made true. If the reader has been selected, then RIN is true and TIN false. This means that R WAIT must go false before $\overline{\text{INBUSY}}$ can go true. This occurs at the end of a tape movement when the load bistable 6/5A/5A is set and L2 goes true.

INSEL and $\overline{\text{INBUSY}}$ being true makes the output of 16/1A go false and set the bistable 16/4A/4A to produce ACT. A 1 μ s delay is introduced before $\overline{\text{ACT1}}$ goes false and triggers the monostable 16/5B/4B to produce 680 ns pulses ACT* and $\overline{\text{ACT*}}$. The 1 μ s delay is produced by the capacitor C1 to earth and prevents small spikes propagating spurious ACT* and ACT** pulses. Another 680 ns pulse ACT** generated by 16/7B sets the bistable 16/2B/2B to send a true [RTR] signal down the interface line.

When $\overline{\text{ACT1}}$ goes false the YES output of 16/7A goes true. INSEL and RIN are also true and hence RDIN goes true and $\overline{\text{RDIN}}$ false. The data is gated onto the interface lines by RDIN.

With ACT* and RDIN both going true the load bistable 6/5A/5A is reset and L2 goes false. R WAIT therefore goes true and $\overline{\text{INBUSY}}$ false to inhibit further $\overline{\text{INSEL}}$ signals until the reader has completed its transfer cycle.

$\overline{\text{RDIN}}$ going false prevents the reader clutch solenoid being energised.

1.4.5.2 Tape Movement

When the central processor has accepted the data on the interface lines, [STR] goes false. SELECT, therefore, goes false and resets the timing chain bistables 16/4A/4A and 16/2B/2B. INSEL going false and $\overline{\text{ACT1}}$ true causes RDIN to go false and $\overline{\text{RDIN}}$ true. All inputs to the tape drive gate 5/2B are now true and $\overline{\text{CLUTCH}}$ goes false to energise the solenoid.

Tape is advanced until a sprocket hole is detected when $\langle\ \overline{\text{SPKT}}\ \rangle$ goes false and triggers the 30 μ s monostable 6/1B/1A. At the same time data signals from the tape should have become false. The 30 μ s pulse forms a delay to ensure that in cases of skewing and worst case circuit tolerance this condition is achieved.

At the end of the delay the bistable 6/2A/3A is set and this triggers the monostable 6/2B/2A. The output is R/S, a 330 ns pulse used to reset the buffer register.

The pulse is also gated with $\overline{\text{RDIN}}$ and $\overline{\text{L2}}$, which are both true, to trigger a monostable 6/3B/4A and produce a 600 μ s GATE pulse to enter data into the buffer register.

The trailing edge of the GATE pulse produces a 330 ns pulse from 2B to set the load bistable 6/5A/5A. $\overline{\text{L2}}$ going false and L2 true. $\overline{\text{L2}}$ causes $\overline{\text{CLUTCH}}$ to go true and the tape movement is stopped. L2 causes R WAIT to go false and allow the next $\overline{\text{INSEL}}$ signal to be accepted.

1.4.6 Operators Controls

1.4.6.1 Hold-Up Lamp

This is lit each time a reader input is demanded, both $\overline{\text{INSEL}}$ and TIN being false. The lamp remains lit until data transfer is completed and $\overline{\text{INSEL}}$ goes true.

1.4.6.2 Read Button

The Read button is operated to load the reader after a new tape has been fitted or to restart after the Stop button has been pressed. Operation of the Read button causes $\overline{\text{LOAD}}$ to go false and this signal is used for three functions.

The bistable 5/2A/3A is set and the output goes true. This causes the Stop lamp to go out and also applies a true signal to gate 5/2A controlling R WAIT.

The pulse generator 5/1B is triggered and LOAD*, a 220 μs pulse, is produced.

$\overline{\text{LOAD}}$ and LOAD* are applied to the bistable 6/7A/6A and as UNLOAD is false due to Tape Out switch being closed, the bistable is set and $\overline{\text{UNLOAD*}}$ goes true. This causes the Read lamp to go off and $\overline{\text{UNL}}$ to go true. $\overline{\text{UNLOAD*}}$ applied to the tape drive gate 5/2B causes $\overline{\text{CLUTCH}}$ to go false and tape movement to start. Tape is advance until a sprocket hole is detected and $\langle \overline{\text{SPKT}} \rangle$ goes false. The action is then as previously described in Sec. 1.4.5.2.

The HOLD signal is set false when $\overline{\text{CLUTCH}}$ is true and this ensures that the bistable 6/7A/6A is not reset when $\overline{\text{LOAD}}$ goes true on releasing the Read button.

1.4.6.3 Stop Button

This button is operated when it is required to stop tape being read. Operation of the button applies a false signal to reset the bistable 5/2A/3A and causes the Stop lamp to light. The false signal from 5/3A11 is also applied to 5/2A5 so that R WAIT is held true preventing an $\overline{\text{INSEL}}$ signal from being accepted. If a reader input is in progress when the Stop button is pressed, the cycle will be completed.

1.4.6.4 Run Out Button

The button allows tape to be run through the reader at full speed independently of the central processor. Operation of the button causes $\overline{R/O}$, the output of 5/4A11, to go false which causes UNLOAD to go true. $\overline{R/O}$ applied to 5/3B1 causes $\overline{CLUTCH}$ to go false and tape movement to commence.

UNLOAD going true resets the bistable 6/7A/6A causing $\overline{UNLOAD*}$ and $\overline{UNL}$ to go false and the Read lamp to light. $\overline{UNL}$ resets the bistable 6/5A/5A and holds $\overline{L2}$ true during the run-out period.

Tape movement continues until the Run-Out button is released and $\overline{R/O}$ goes true. The Read button must be operated to set the bistable 6/7A/6A before reading can restart.

1.4.7 Error Conditions

1.4.7.1 Tape-Out Switch

This is a micro-switch located beneath the tape guide plate on the reader. It is operated when the plate is raised for loading or unloading of tape and when the end of the tape passes through the plate.

Release of the switch applies a false signal to 5/4A and causes UNLOAD to go true. This is turn resets the bistable 6/7A/6A causing $\overline{UNLOAD*}$ to go false and the Read lamp to light. $\overline{UNLOAD*}$ prevents $\overline{CLUTCH}$ going false to move the tape, and R WAIT going false to accept an $\overline{INSEL}$ signal.

1.4.7.2 Creep Error

This occurs when the tape does not stop quickly enough and a second SPKT pulse is detected. The 30 μ s DELAY pulse is gated with L2, and when both are true, a false signal is obtained from 6/4A13. This signal is mixed with $\overline{UNLOAD*}$ the output of 6/7A13 and resets the bistable 6/7A/6A to prevent further reading of the tape.

1.4.7.3 Hold

This signal is normally held at a false level by the output of gate 5/2B which has the same sense as $\overline{\text{CLUTCH}}$. When a tape movement is initiated, after a data transfer, the output of 5/2B goes false and the input to the regenerable monostable 5/4B goes true. The monostable has a recovery time of 200 ms and if a sprocket hole is not detected and the tape movement stopped within that period, then HOLD will go true. This causes the bistable 6/7A/6A to reset and the Reader to unload.

This condition can occur if the end of the tape has passed the read head, unpunched tape is passed through the reader, or if the tape is caught and prevented from moving.

1.5 Paper Tape Output Logic

1.5.1 Introduction

This section contains a functional description of the logic associated with the paper tape punch. The logic is shown in Figs. C20, C22 and C23.

1.5.2 Basic Operation

1.5.2.1 Typical Cycle

Assuming the motor is running, a brief description of the normal cycle of events is as follows:

On receipt of an output signal, a timing sequence is initiated which gates the data from the interface lines into a buffer and then sends a reply to the central processor.

The punch cycle commences on receipt of a synchronising pulse from the punch mechanism. This causes the data solenoids, and approximately a millisecond later, the feed solenoid to be energised. The data holes are punched and the tape advanced to the next character position. The buffer is cleared and the punch is then ready to receive the next output signal.

1.5.2.2 First and Last Cycle

To avoid excessive wear, the punch motor is only switched on when it is required to perform a punching operation.

The motor is switched on by the first data output transfer and a one second delay is introduced to allow the motor to attain full speed before punching commences.

On completion of the last data output transfer, a period of five seconds is allowed before the motor is switched off.

1.5.3 Channel Selection

An output to the tape punch is selected according to the position of the Select Output switch and/or the type of system in use. (This is accomplished by operating the necessary controls on the Teleprinter and Paper Tape Controller. (Fig C19 and Fig. h refer). For an output to be sent to the punch POUT must be true.

If a teleprinter is not used its associated logic is omitted and the T/P Link on board 22 will not be present. This holds the input to gate 14/4B at a true level and means that TOUT is always false and POUT always true. The position of the Select Output switch has no effect on the logic.

When a teleprinter is used TOUT will be false and POUT true if the Select Output switch is set to PUNCH or AUTO with the interface signal [ADDRESS BIT 3] false. TOUT will be true and POUT false if the Select Output switch is set to TELEPRINTER or AUTO with the interface signal [ADDRESS BIT 3] true.

1.5.4 Data Flow

Data to the punch in the form of an eight-bit character is present on the interface lines [OP1] to [OP8] when an [STP] signal is sent from the central processor.

At the end of a data output and when the equipment is first switched on, the BUFF R/S signal from 11/6A12 resets the buffer bistable 10/1A/1A etc., such that the outputs 10/1A12 etc., are true.

$\overline{\text{PD OUT}}$ is inverted by 10/4B13 and 10/5B12 and then gated with the data lines $\overline{\text{OUT1}}$ etc., the bistable outputs 10/1A12 etc., being left true if the corresponding data line is false, and being set false if the data line is true. $\overline{\text{PUNCH*}}$ is inverted by 10/5B13, gated with the outputs of the above bistables at 10/2B etc., the appropriate punch solenoids being energised.

$\overline{\text{PUNCH*}}$ is derived from the monostable 11/2B/4A which is triggered on receipt of a true < SYNC > pulse from the motor mechanism. The false $\overline{\text{FEED}}$ pulse is effectively the same as $\overline{\text{PUNCH*}}$ but is delayed by one millisecond. At the end of $\overline{\text{PUNCH*}}$ the BUFF R/S pulse is generated by monostable 11/5B/6A to reset the buffer bistables.

1.5.5 Punch Timing

1.5.5.1 Data Transfer

When a data transfer is required, interface signal [STP] is made true. If the punch is selected then POUT is true and TOUT false. This means that P WAIT must go false before $\overline{\text{OUTBUSY}}$ can go true. This occurs at the end of a punching operation when the bistable 12/4A/4A is reset and $\overline{\text{L}}$ goes true.

OUTSEL and $\overline{\text{OUTBUSY}}$ being true makes the output of 16/1A go false and set the bistable 16/4A/4A to produce $\overline{\text{ACT}}$. A 1 μ s delay is introduced before $\overline{\text{ACT1}}$ goes false and triggers the monostable 16/5B/4B to produce 680 ns pulses ACT* and $\overline{\text{ACT*}}$. The 1 μ s delay is produced by the capacitor C1 to earth and prevents small spikes propagating spurious ACT* and ACT** pulses. Another 680 ns pulse ACT** generated by 16/7B sets the bistable 16/2B/2B to send a true [RTR] signal down the interface line.

When $\overline{\text{ACT1}}$ goes false the YES output of 16/7A goes true. ACT* goes true for 680 ns and as OUTSEL and POUT are also true then $\overline{\text{PDOUT}}$, from 16/6B12, will go false for 680 ns. This pulse gates the data from the interface lines into the buffer bistables 10/1A/1A etc., and also sets the bistable 12/4A/4A causing $\overline{\text{L}}$ to go false and L true.

With $\overline{\text{L}}$ going false P WAIT goes true and $\overline{\text{OUTBUSY}}$ false to inhibit further $\overline{\text{OUTSEL}}$ signals until the punch has completed its punching cycle.

1.5.5.2 Motor Timing

When $\overline{\text{L}}$ goes false the output of 12/4A13 (the OK signal) goes true. The OK signal is used to trigger the 5-second regenerable monostable 12/3B and the 100 ms pulse generator 12/5A/5B.

Assume that no data transfer has taken place for at least 5 seconds then, on the first transfer OK will have been false long enough for the output of regenerable monostable 12/3B to have returned to a false level. Thus SCR will be true, the bistable 12/1B/1B will be reset and MOTOR ON false.

The OK signal going true causes the output of 12/3B to go true and hence SCR will go false switching mains power to the punch motor.

The 100 ms pulse from 12/5B triggers the 1 second regenerable monostable 12/2B. When the monostable recovers the output becomes false and the 50 μ s pulse generator 12/4B is triggered. This pulse sets the bistable 12/1B/1B causing MOTOR ON to go true and enable punching to proceed.

The motor remains switched on with SCR false and MOTOR ON true until $\overline{L}$ has been true for at least 5 seconds. If $\overline{L}$ goes false within the 5 second period then the above state will continue for a further 5 seconds. Note also that $\overline{R/O}$ has the same effect as $\overline{L}$.

1.5.5.3 Punching Signals

A synchronising pulse ⟨ SYNC ⟩ occurs once per cycle of the motor and from it the punch and feed signals are derived.

When the ⟨ SYNC ⟩ pulse occurs the monostable 11/1B/2A is triggered and a 40 μ s pulse produced. If at the same time, MOTOR ON and OK are true, the output of gate 11/3A goes false to trigger the monostable 11/2B/4A. The output on 11/4A13 is $\overline{\text{PUNCH}}$ which goes false for a period of 5 ms. This causes $\overline{\text{PUNCH*}}$ to go false also for 5 ms to energise the solenoids in the punching mechanism. A description of the solenoid driver board is contained in Section 1.6.

The 1 ms monostables 11/4B/3A and 11/3B/2A together with gates 11/4A and 11/5A produce $\overline{\text{FEED}}$ which is identical to $\overline{\text{PUNCH*}}$ but delayed by 1 ms. When $\overline{\text{PUNCH}}$ goes false the 1 ms monostable 11/4B/3A is triggered, the false output on 11/3A11 holding $\overline{\text{FEED}}$ true. At the end of the 1 ms period both inputs to gate 11/5A are true and $\overline{\text{FEED}}$ goes false to commence movement of the tape. When $\overline{\text{PUNCH}}$ returns to true the monostable 11/3B/2A is triggered and this maintains the true input to gate 11/5A for 1 ms.

Also when $\overline{\text{PUNCH}}$ returns to a true level, the monostable 11/5B/6A is triggered causing BUFF R/S to go true for 470 ns. This pulse is used to reset the data buffer bistables and the bistable 12/4A/4A causing $\overline{\text{L}}$ to go true. This means P WAIT goes false and the punch is ready to accept the next $\overline{\text{OUTSEL}}$ signal.

1.5.6 Operators Controls

1.5.6.1 Reload Button

This button is operated to override a tape low condition or after a new reel of tape has been fitted into the punch.

Operation of the button applies two false inputs to reset the bistable 12/2A/2A. This causes $\overline{\text{LOW}}$ to go true and extinguish the Reload lamp.

If the button is held down, then a tape low condition can be overriden.

1.5.6.2 Run-Out Button

This button is operative at all times and causes the punch to continuously output blank tape.

Operation of the button causes $\overline{\text{R/O}}$ to go false and this holds OK and therefore MOTOR ON at a true level. All $\langle$ SYNC $\rangle$ pulses from the motor mechanism will be accepted and a series of $\overline{\text{FEED}}$ pulses produced.

With the false $\overline{\text{R/O}}$ signal applied to 11/2A, then P WAIT is held true and $\overline{\text{OUTSEL}}$ signals cannot be accepted. Thus $\overline{\text{PDOUT}}$ remains true and the bistable 12/4A/4A remains reset with L false. The L signal applied to 11/6A holds $\overline{\text{PUNCH}}$* at a true level and prevents any data holes being punched.

1.5.7 Error Conditions

1.5.7.1 Tape Low

This is a microswitch which closes when the supply of tape on the spool is nearly exhausted.

Closing of the contacts applies a true signal to set the bistable 12/2A/2A causing $\overline{\text{LOW}}$ to go false and the Reload lamp to light. With $\overline{\text{LOW}}$ held false P WAIT is held true and no $\overline{\text{OUTSEL}}$ signals can be accepted by the punch. If the Reload button is held down, the error condition can be over-ridden.

1.5.8 Reset Signals

1.5.8.1 I. RESET

This is a true pulse which is generated within the paper tape station from 15/6A13 when the equipment is first switched on. The pulse is used to ensure that SCR remains true during this period and the motor is not switched on.

1.5.8.2 $\overline{\text{RESET}}$

This signal from 15/7A13 is derived from the [RESET] signal generated in the central processor. The signal goes false when the equipment is first switched on and also when the Reset button is operated. The signal remains false until the Jump button is pressed.

$\overline{\text{RESET}}$ going false causes BUFF R/S to go true and reset the data buffer bistables 10/1A/1A etc.

1.6. Reader/Punch Drivers

1.6.1 Introduction

The Reader/Punch Driver board is a type DPS13 and is located in position 4 of the logic rack. The board contains eleven solenoid driver circuits, nine for the punch, one for the reader and one spare. A common under-voltage protection circuit is also provided for all but the spare driver circuit. The protection circuit prevents operation of the drivers when either the +6V or +28V d. c. supplies are low. If one or both of these supplies is low, the drive circuit may not operate correctly and hence cause malfunction of the punch or reader. The layout of the components on the printed circuit board is shown in Fig. C25.

1.6.2 Under-Voltage Protection Circuit

A circuit diagram is shown in Fig. C25. When the equipment is first switched on and before the d. c. power rails have reached their operating levels, VT1 is reverse biased and VT2 conducting. As the +28V rail rises in level, current flows through R1, R2, MR2, MR3 and R3 until the junction of R2 and MR2 is at a high enough potential to cause MR1 to perform its zener function. This occurs when the d. c. rail reaches approximately 15V, the zener voltage is 4. 7V. The d. c. level on the base of VT1 falls to around 3. 3V. Therefore when the +6V rail rises to approximately 4V, VT1 will conduct causing VT2 to cut off.

During operation of the equipment if the +6V level falls to below 4V then VT1 will be reverse biased and VT2 will conduct. Similarly, if the +28V level falls sufficiently to prevent MR1 from performing its zener function, the level on the base of VT1 rises causing the transistor to cut off and VT2 to conduct.

1.6.3 Driver Circuit

A circuit of the driver is shown in Fig. C25. There are eleven circuits, ten of which are connected via the diodes MR1 to the under-voltage protection circuit. If the d. c. rails are at a satisfactory working level then a false input signal to the drive circuit causes the level on the base of VT1 to fall and the transistor to conduct. The level on the base of VT2, therefore, rises, the transistor conducts, and the solenoid is energised. A true input to the circuit holds VT1 and VT2 in the off state.

The diode MR4 is to suppress the voltage surge generated during the switch off period.

1.6.4 Action of Protection Circuit

The collector of VT2 in the protection circuit is connected to the cathode of MR1 in ten of the drive circuits. When either or both of the d. c. supplies are low, VT2 in the protection circuit is conducting. If the input to the drive circuit goes false, diode MR1 in the drive circuit is forward biased and this will prevent VT1 from switching on.

When the d. c. rails have reached a satisfactory level, VT2 is reverse biased. If the input to the drive circuit now goes false, diode MR1 is reverse biased and hence the level on the base of VT1 will fall and cause the drive circuit to energise the solenoid.

1.7 Maintenance and Test Programs

1.7.1 Introduction

These instructions are intended to supplement and not replace the Maintenance Instructions detailed in the Manufacturer's handbooks, which should still be followed as closely as possible.

The instructions are divided into two categories.

Class I should be carried out at four weekly intervals if the system contains line printers, magnetic tapes or data discs, otherwise it may be carried out every six weeks. These periods are based on an average working day of eight hours. If the equipment is consistently used for longer than eight hours per day, maintenance should be carried out more frequently.

Class II is subject to the same provisions as Class I, but is based on a twelve-weekly period.

1. 7. 2 Tape Punch

1. 7. 2. 1 Introduction

The punch will retain its accuracy and reliability if it is properly maintained. Although it will perforate tape at high and low speeds, the operating life is increased if operated at low speeds.

1. 7. 2. 2 Class I Maintenance

(1) The punch should be thoroughly cleaned with a lint-free cloth to remove dust and grease accumulations. A brush may be used to reach inaccessible areas. Care should be taken to avoid damage to delicate parts of the instrument.

(2) Check that all wiring is intact and securely terminated.

(3) Ensure that nuts and screws are tightened, and locked if required.

(4) Inspect the instrument for signs of deterioration or wear which may cause trouble at a later date.

(5) Check the clearance between adjacent moving parts and for any signs of insufficient lubrication.

(6) Check that all data holes and the feed hole are clearly punched. If this check is not satisfactory, the punching block and punching mechanism should be inspected.

(7) Using the paper tape gauge, ensure that the feed holes are correctly related to the guiding edge of the tape, the slot in the gauge lying centrally over the holes.

(8) Rotate the flywheel and check that the feed pawl is not under or overthrowing the feed wheel.

(9) Check that the tape reel brake is operating satisfactorily.

(10) Lubricate all parts as detailed in the manufacturer's handbook.

1. 7. 2. 3 Class II Maintenance

(1) Carry out Class I Maintenance.

(2) Check that the tape low contacts close when approximately 0. 5 inch thickness of tape remains on the spool. Adjust as necessary.

(3) Check that all armatures are attracted to the pole pieces when their solenoids are energised. With the armature in the attracted position, check that the gap between the armature and the pole piece is within the limits 0.003 to 0.001 inch at the point of least clearance.

(4) Ensure that the clearance between the blocking pawls and the long toggle arms is within the limits .003 to .002 inch.

1.7.3 Tape Reader

1.7.3.1 Introduction

The reader is an electro-mechanical device designed to provide high speed input for computer processors. The maximum rated speed is 250 characters per second.

The device is highly reliable and accurate, and can be made to retain these qualities if properly maintained.

1.7.3.2 Class I Maintenance

(1) Clean the outside of the reader.

(2) Clean the bulb, prism and window with an anti-static cloth. Replace the bulb if the filament is broken or the glass envelope is discoloured. Check the prism for scratches or crazing

(3) Check that the tape guides have not been scored by the tapes.

(4) Using a small stiff brush remove any dust, etc., from the brake assembly.

(5) Using gauge D4/22/A206 ensure that the two adjustable tape guide posts can be correctly positioned for all widths of tape.

(6) Check that the light pattern thrown on the holes under the prism is of the correct size and shape. There should be a lighted area which is wider than the holes and has roughly parallel sides evenly disposed about the holes.

(7) Check that the gap between the pinch roller and capstan is 0.0065 to 0.007 inch.

(8) Check that the brake pad is 0.002 to 0.004 inch above the top plate.

(9) Check that the clutch pressure is 320 to 360 gm. Check that the standing brake pressure is within the limits 45 to 55 gm.

(10) Check that all nuts and screws are tight.

(11) Lubricate threads of Plessey plugs with a light grease.

(12) Lubricate all parts as detailed in the manufacturer's handbook.

(13) Check the waveform of the sprocket and data hole outputs. Details are contained in the manufacturer's handbook.

(14) Inspect the hand spooler and ensure the rim is smooth.

1. 7. 3. 3 Class II Maintenance

(1) Carry out Class I Maintenance.

(2) Check that the pinch rollers and capstan are parallel within 0. 0005 inch and that the end float on the pinch roller is between 0. 006 and 0. 009 inch. Check that the roller is not worn and rotates freely.

(3) Inspect the upper and lower brake pads for wear. Any sign of grooving by the tape should be removed by machining or stoning flat or by replacement of the pads.

(4) Check, using an Avometer, that the lamp voltage is 9. 2V ± 0. 5V.

(5) With no tape in the reader, energise the clutch and check that the gap between the pinch roller and capstan is 0. 001 to 0. 002 inch.

(6) Check the power unit outputs. They should be within:

5. 5V to 6. 5V (two supplies)

and 23. 8V to 32. 2V

all for a mains input of selected voltage ± 10%

1.7.4 Setting-Up a Punch

1.7.4.1 Punching a Full-House Tape

(1) Ensure that the MODE switch is set to TEST.

(2) Set the eight least significant keys of the word generator to the '1' position.

(3) Set the ENTER key to the up position and return to centre position.

(4) Set the word generator keys to 15 6144.

(5) Operation of the OBEY key will cause the punch to produce a full-house tape. The key has three positions, the centre one being normal or off. In the up position, a full-house is punched for each operation of the key and in the down position the punch continuously produces full-house tape.

1.7.4.2 Spring Adjustments

(1) Set the equipment to produce a full-house tape from the punch as described in Section 7.4.1

(2) Loosen the armature restoring spring locknuts on the code 1 magnet. Tighten the spring carefully until the code 1 hole is just not punched. Tighten the locknuts and ensure that the code hole is still not punched.

If on tightening the spring, maximum tension is reached and the code hole is still punching, tighten the locknuts for maximum tension and omit the adjustment in sub-paragraph (5).

(3) Repeat sub-paragraph (2) for the other seven code magnets.

(4) Loosen the locknuts on the feed magnet armature restoring spring. Tighten the spring to maximum tension. If tape is not being fed through the punch, slacken the spring carefully until tape is just being fed. Give the spring adjusting nut one complete turn in the direction to slacken the spring, then tighten the locknuts.

(5) Loosen the locknuts on the armature restoring spring of the code 1 magnet. Slacken the spring carefully until code hole 1 is just punched. Check that the hole is also punched under stop/start conditions. Tighten the locknuts.

(6) Repeat sub-paragraph (5) for the other seven code magnets, ensuring that a full-house is being punched.

(7) Slacken the locknuts on the armature restoring spring of the code 1 magnet. Give the spring adjusting nut one complete turn in the direction to slacken the spring, then tighten the locknuts.

(8) Repeat sub-paragraph (7) for the other seven code magnets.

(9) On completion of these adjustments, the punch mechanism should be lubricated as detailed in the manufacturer's handbook.

1.7.5 Test Program

A diagnostic program is not provided for the paper tape station. On completion of Class I or Class II Maintenance, the operators daily test program X51 should be run to ensure the correct functioning of the equipment. Satisfactory working for approximately half a reel of tape, ensures that the equipment is in a working state. X51 is described in the Test Program Library Cat. No MCB 145.

2. TELEPRINTER

2.1. Introduction

2.1.1 Location of Component Parts

The teleprinter is a type 33 which is mounted on its own stand and usually positioned by the side of the central processor desk. The teleprinter incorporates a reader and punch, which will be called the printer reader and printer punch, to avoid confusion with the tape reader and tape punch which may be used in conjunction with the teleprinter.

The power supply unit, with its associated control circuitry, and the rack containing the logic boards are mounted in the left hand side of the processor desk. The operators' controls are located on the teleprinter and on a rack mounted panel.

A typical assembly of the component units is given in Fig. C15. For teleprinter operation logic boards 4 to 12 inclusive are not used.

2. 1. 2. Logic Boards

The circuits of the L. S. A. elements used on the logic boards are described in Section 1 of this Part of the Manual. The tables in Fig. C31 provide details of the types of L. S. A. element on each board and the location and value of any extra components used.

Descriptions of the special circuits located on board DPS 14, in position 25 of the logic rack, are contained in Section 2. 6.

On the logic diagrams Figs. C28, C29 and C30, signals to and from the central processor are enclosed in square brackets [ ] and signals to and from the teleprinter are enclosed in diamond brackets < >. All discrete components, not being part of the sub-assemblies, are fitted in Area G of the logic board. Fig. g refers.

2. 2. Interconnections

Interconnections within the Paper Tape Station, Computer, Teleprinter and Power Supply are given in Fig. C16.

2. 2. 1 Interconnections between Control Station Power Supply and Teleprinter

CONTROL STATION POWER SUPPLY TO TELEPRINTER

19-TB1 TO 20-TBB		FUNCTION
7	1	Line
8	3	Neutral
9	2	Earth

2. 2. 2 Interconnections between Logic Rack and Teleprinter

LOGIC RACK TO TELEPRINTER

18-CND TO 20-TBA		FUNCTION
A	7	T/P Line Transmitter
B	6	T/P Line Receiver
C	3	-

2. 3 Power Distribution

2. 3. 1 Introduction

The power distribution is shown in Figs. C26 and C27. The control station is wired so that it can accommodate the teleprinter plus a tape punch and tape reader. When a full system is not used, the logic boards associated with the missing devices are omitted. The Figures in this section show the complete wiring and are not isolated to that used by the teleprinter.

2. 3. 2 A. C. Supplies

The distribution of the a. c. supplies is shown in Fig. C26.

The mains input on TB1 is taken to the contacts of RLA. This relay is energised by a 24V signal from the interface which is present when the mains ON button on the control unit is operated. A Local/Remote switch is available to by-pass the relay contacts when required.

2. 3. 3 D. C. Supplies

The distribution of the d. c. supplies is shown in Fig. C27.

The d. c. supplies are produced by two units labelled PSA and PSB.

PSA is a type NS-ELL/006 and provides the +6V and -6V supplies at current ratings of 3A and 1A respectively. PSB is a type ES 1000/28, and provides the +28V supply at a current rating of 10A.

Details of these units can be obtained from the manufacturer's handbooks.

2.3.4 Over-Voltage Protection

An over-voltage protection circuit is connected across the +6V and -6V d.c. outputs to protect the logic boards from damage due to a rise in level of either of these supplies. Under normal operating conditions, the lamps will be lit and no current taken by the circuit.

If either of the d.c. outputs start to rise then current will be drawn through the corresponding Zener diode and current applied to the thyristor. Dependent on the ambient temperature and component tolerances, the thyristor will be triggered when the d.c. level has risen to a value between 6.5V and 10.0V.

When the thyristor conducts, the output terminals of the power unit are short circuited causing the appropriate fuse to blow and extinguish the lamp.

2.4. Teleprinter Input

2.4.1 General

The teleprinter used is a type 33 (MCB 66D) which rests on its own stand. The teleprinter incorporates a reader and punch which will be called the printer reader and printer punch, to avoid confusion with the tape reader and tape punch which may be used in conjunction with the teleprinter.

This section contains a functional description of the control logic associated with the teleprinter when used to input a character into the central processor. The character can originate from the keyboard or the printer reader, in either case a common input line carries the information to the logic, Figs. C28 and C29 refer.

2.4.2 Basic Cycle

A brief description of the normal transfer cycle when the teleprinter is not busy is as follows:

On receipt of an input selection signal the Demand lamp lights. When a key is pressed or the printer reader started, a serial character is produced and fed to the logic. The first pulse of the character is used as a starting signal for a clock which produces pulses to cause the character to be loaded in serial mode into a buffer register. The character is also fed back to the teleprinter to operate the typing mechanism and, if required, the printer punch.

When the character is in the correct position in the buffer the clock is stopped and further characters from the teleprinter inhibited. The input selection signal is now accepted by the interface logic and a timing sequence initiated to gate the data from the register onto the interface lines.

After the data has been accepted by the central processor, the input selection signal is removed, the Demand lamp goes out, and the logic is reset ready to accept the next data transfer.

2.4.3 Channel Selection

An input from the teleprinter is selected according to the position of the Select Input switch and/or the type of system in use. (This is accomplished by operating the necessary controls on the Teleprinter and Paper Tape Control Unit). Figs. C19 and Fig. h refer. For an input to be taken from the teleprinter, TIN must be true.

If a tape reader and tape punch are not used, the associated logic is omitted and the READ and PUNCH LINKS on boards 5 and 11 respectively will not be present. This means that the inputs to 14/1B11 and 14/1B12 are at a true level and will always hold TIN true and RIN false. Under these circumstances the position of the Select In switch has no effect on the logic and all inputs must come from the teleprinter.

When a tape reader and tape punch are used with the system, the READ and PUNCH LINKS are present. In this case TIN will be true and RIN false when the Select In switch is set to TELEPRINTER, or to AUTO with the interface signal [ADDRESS BIT-3] true. At all other times TIN will be false and RIN true.

2.4.4. Character from Teleprinter

A character from the teleprinter, whether derived from the keyboard or the printer reader, is approximately 100 ms long when the teleprinter is operating at 10 characters per second and consists of eleven pulses.

The character is sent to the logic in serial form, and when viewed at the output of the line receiver 23/6B12, the first pulse is always true and is called the Start pulse. The next eight pulses contain the code of the character and may be either true or false according to the code combination. The last two pulses are always false and are called the Stop pulses. The output then remains false until the next character is sent.

2.4.5. Teleprinter Clock

2.4.5.1 Clock Pulses

The clock pulses $\overline{S1}$ and $\overline{S2}$ are used to strobe the data along the register during both input and output modes of operation. The timing is arranged so that $\overline{S1}$ and $\overline{S2}$ are produced alternately with a period of 4.55 ms between each pulse. The timing of the clock is shown in Fig. C30.

The logic for the clock is located in DPS14 and DP18 in positions 25 and 23 respectively of the logic rack and is shown in Fig. C30.

2.4.5.2 Initial Conditions

When a data transfer is not in progress the clock is not running and all inputs to 25/2B12 are at a true level. This causes the output to be false and hence CLOCK BUSY, (the output of 23/6A13) is also false.

The bistable 23/3A/2A is set by the false output of the pulse generator 23/3B11 and CLOCK BUSY such that the output of 23/3A12 is true.

2.4.5.3 Operation of Clock

The conditions required for the clock to start are that all inputs to 25/2A12 must be true, causing the output to go false. This triggers the pulse generator 25/3A11 to produce a 330 ns pulse to open gate 25/4A12 and cause $\overline{\text{TIME1}}$ to go false. $\overline{\text{TIME1}}$ is inverted by 25/4A13 and used to fire the special pulse generator which produces an accurate 2.27 ms pulse. This pulse applied to 25/4A12 holds $\overline{\text{TIME1}}$ at a false level for 2.27 ms.

$\overline{\text{TIME1}}$ fed to 25/2B12 causes CLOCK BUSY to go true.

$\overline{\text{TIME1}}$ is also inverted by 25/2A11 and applied to the pulse generator 25/3A13. At the end of $\overline{\text{TIME1}}$ this pulse generator is triggered and a 330 ns pulse produced. This is the COUNT pulse and is used for two purposes.

The COUNT pulse is applied to 25/4B12 to cause $\overline{\text{TIME2}}$ to go false. $\overline{\text{TIME2}}$ is held false by 25/4B13 and the special 2.27 ms pulse generator.

The COUNT pulse is inverted by 23/2B11 and applied to the two pulse generators 23/3B11 and 23/3B13. The outputs of the bistable 23/3A/2A are also fed to the pulse generators and as the output 23/2A12 is false then 23/3B13 is not triggered. The pulse from 23/3B11 sets the bistable causing the output of 23/3A12 to go false.

$\overline{\text{TIME2}}$ is fed to 25/2B11 and is also used to ensure that CLOCK BUSY remains true. At the end of the 2.27 ms $\overline{\text{TIME2}}$ pulse the output of 25/2B11 goes false to trigger the pulse generator 25/3B13 to produce the 10μ s SHIFT pulse This pulse is gated with the outputs of the bistable 23/3A/2A and $\overline{\text{S1}}$ is produced from 23/2A13.

Shift is also inverted by 25/2A13 and fed to the gate 25/2A12 causing its output to go true. At the end of the SHIFT pulse the output of 25/2A12 goes false to initiate a further cycle of the clock.

During the next cycle the COUNT pulse will trigger pulse generator 23/3B13 to reset the bistable 23/3A/2A such that the output of 23/3A12 is true. The SHIFT pulse will therefore produce $\overline{\text{S2}}$ from 23/3A13.

The clock continues to produce $\overline{\text{S1}}$ and $\overline{\text{S2}}$ pulses until the character shift is complete and RUN goes false. This holds the output of 25/2A12 at a true level and prevents further triggering of the clock.

When the last $\overline{\text{SHIFT}}$ pulse goes true, CLOCK BUSY goes false to reset the bistable 23/3A/2A such that the output of 23/3A12 is true. This ensures that when the clock is restarted, $\overline{\text{S1}}$ will be the first pulse produced.

2.4.6 Teleprinter Input Timing

2.4.6.1 Demand Signal

When a input is required by the central processor, interface signal [STR] goes true and hence $\overline{\text{INSEL}}$ goes false. RIN is false when the teleprinter is selected, and this signal with $\overline{\text{INSEL}}$ causes the Demand lamp to light via the logic element 15/4B. The Demand lamp is located on the control panel.

2.4.6.2 INFO

When a key is pressed or the printer reader is started, a character will be produced by the teleprinter (see Section 2.4.4) and sent in serial fashion to the line receiver 23/6B12.

The two signals $\overline{\text{RESET}}$ and $\overline{\text{BLOCK}}$ are true and the outputs of 23/4B13 and 23/5B11 are both false, holding 23/5A12 true. the Start pulse causes $\overline{\text{INFO}}$ (the output of 23/6A12) to go false. This signal is inverted by 23/5A13 to produce INFO.

In the input mode of operation, the INFO signal is identical to the character generated by the teleprinter mechanism. The signal is reinput to the teleprinter via the line transmitter 23/7B13 to operate the typing mechanism and, if required, the printer punch.

2.4.6.3 Starting the Clock

INFO is gated at 22/2A11 with $\overline{\text{BLOCK}}$ and $\overline{\text{TDOUT}}$, both of which are true, causing the output to go false. This in turn sets the bistable 22/2A/2B causing R to go true and $\overline{\text{R}}$ false.

$\overline{\text{R}}$ going false causes RUN (the output of 22/3B13) to go true. RUN is fed to 25/2A12 which is the gate controlling the running of the clock. The other three inputs are true so that RUN going true causes the output of 25/2A12 to go false and start the clock running. The operation of the clock is described in Section 2.4.5.

$\overline{R}$ is also fed to 22/5A11 causing CLEAR to go false so that data can be loaded into the buffer register.

2.4.6.4 Loading the Register

The register consists of eleven stages, each comprising two bistables, located on boards 19, 20 and 21 of the logic rack. The first of the bistables in each stage is strobed by the $\overline{S1}$ pulse and the second bistable in each stage by the $\overline{S2}$ pulse. The serial characters INFO and $\overline{INFO}$ are fed to 19/1A12 and 19/1A13 respectively and by the strobing action of the clock pulses are moved along the register from left to right.

When the register is not being used, it is held in the reset state by the CLEAR signal being true. This means that the top output of each stage, $\overline{ST}$ on the eleventh stage, is at a true level, and the lower output, ST on the eleventh stage, at a false level.

The character is moved to the right by the strobing action of the clock pulses until the tenth $\overline{S1}$ pulse occurs. At this point the Start pulse of the character will be gated by $\overline{S1}$ at 21/4B12 causing the output to go false. This signal is inverted by 21/4A13 causing STOP I/P to go true.

2.4.6.5 Stopping the Clock

STOP I/P is gated with $\overline{L*}$ and R at 22/1B11 causing the output to go false. This sets the bistable 22/1A/1B causing $\overline{L}$ to go false. $\overline{L*}$ also goes false to reset the bistable 22/2B/2A causing $\overline{R}$ to go true and R false. With $\overline{R}$ going true, RUN goes false and inhibits further start pulses for the clock at 25/2A12.

$\overline{L}$ applied to 22/4B12 and $\overline{R}$ applied to 22/5B11 causes BLOCK (the output of 22/5B12) to go true. $\overline{BLOCK}$ (the output of 22/5B13) applied to 23/6A12 holds its output at a true level. If a key is pressed the character is inhibited at 23/6A12 by $\overline{BLOCK}$ and also gated with BLOCK at 23/4A12 causing the output to go false. This false output triggers the pulse generator 23/4B13 and causes the output of the regenerable monostable 23/5B11 to go true. These signals cause the output of 23/5A12 to go false and enforce the inhibit on 23/6A12. The regenerable monostable has a recovery time of 200 ms, so that this period must elapse after BLOCK has gone false before a character is allowed to pass to the INFO state.

$\overline{BLOCK}$ also inhibits any spurious INFO signals at 23/7B13 and 22/2A11.

$\overline{L}$ going false and applied to 22/5A12 ensures that CLEAR remains false and the register is not reset.

When R goes false, the pulse generator 23/1A13 is triggered, the resultant 10 ms pulse is used to inhibit spurious pulses to the teleprinter from the $\overline{ST}$ line at 23/1B12. The pulse in inverted by 23/1B13 to produce $\overline{INH}$. This pulse is applied to 25/2A12 to prevent the clock from starting, and to 22/3B12 to hold T WAIT true.

2.4.6.6 Data Transfer

As RUN, CLOCK BUSY and $\overline{L}$* are false, when $\overline{INH}$ goes true at the end of the 10 ms pulse, T WAIT goes false.

With the teleprinter selected RIN is false and TIN true, so that T WAIT going false causes $\overline{INBUSY}$ (the output of 16/2A12) to go true. As INSEL is true the output of 16/1A12 goes false to set the bistable 16/4A/4A causing $\overline{ACT}$ to go false. A 1 μ s delay is introduced before $\overline{ACT1}$ goes false and triggers the monostable 16/5B/4B to produce 680 ns pulses ACT* and

$\overline{\text{ACT*}}$. The 1 μ s delay is produced by the capacitor to earth and is to prevent small spikes propagating spurious ACT* and ACT** pulses. The 680 ns pulse ACT** generated by 16/7B13 sets the bistable 16/2B/2B to send a true [RTR] signal down the interface line.

$\overline{\text{ACT1}}$ is inverted by 16/7A12 to produce YES which is in turn gated with TIN and INSEL to give a false $\overline{\text{TDIN}}$ signal from 15/2B11 and a true TDIN signal from 15/1B11.

ACT* and TDIN applied to 22/1A12 causes $\overline{\text{RESETL}}$ to go false for 680 ns to reset the bistable 22/1B/1A causing $\overline{\text{L}}$ and $\overline{\text{L*}}$ to go true. BLOCK is held true and CLEAR false by $\overline{\text{TDIN}}$ applied to 22/4B12 and 22/5A12 respectively. $\overline{\text{L*}}$ applied to 22/3B11 causes T WAIT to go true

When the input to the register was stopped the data is present on the outputs of the left hand eight stages of the register. The data is applied to the gates 1A etc., on board 15 and when TDIN goes true this data is strobed onto the interface lines [IR1] to [IR8] via the line transmitters 14/1A11 etc.

After the data has been accepted by the central processor, [STR] goes false causing SELECT (the output of 16/1A13) to go false and reset the bistable 16/4A/4A and 16/2B/2B. $\overline{\text{ACT1}}$ goes true causing $\overline{\text{TDIN}}$ to go true.

With $\overline{\text{TDIN}}$ going true, CLEAR goes true to reset the buffer register, and BLOCK goes false to enable a further character to be input.

2.4.7 Reset Signals

2.4.7.1 $\overline{\text{RESET}}$

This signal from 15/7A13 is derived from the [RESET] signal generated in the central processor. The $\overline{\text{RESET}}$ signal goes false when the equipment is first switched on and also when the Reset button

is operated. The signal remains false until the Jump button is pressed.

The $\overline{\text{RESET}}$ signal has four uses.

(1) Applied to bistable 22/1B/1A it ensures that $\overline{L}$ is true.

(2) Applied to bistable 22/3A/3A it ensures that $\overline{O}$ is true.

(3) Applied to 22/2B11 it ensures that the bistable 22/2B/2A is set such that $\overline{R}$ is true.

(4) Applied to 23/6A12 it ensures that INFO is held false.

2.4.7.2 $\overline{\text{RESET}}$

This in the inverse of $\overline{\text{RESET}}$ and is obtained from 15/7A11. It is applied to 22/5A11 to hold CLEAR true and the register in a reset state.

2.5. Teleprinter Output

2.5.1. Introduction

This section contains a functional description of the control logic associated with the teleprinter when used as an output device for a character from the central processor. The logic is given in Figs. C28 and C29. The character is typed by the keyboard printer, and if required, can be reproduced on tape by the printer punch.

2.5.2. Basic Cycle

The following is a brief description of the normal transfer cycle provided that the teleprinter is not busy.

The teleprinter logic accepts the output selection signal from the central processor and starts a timing chain which gates the data into the buffer register and sends a reply to the processor.

When the output selection signal is removed, the clock is started and a series of strobing pulses produced. These pulses shift the character to the right and it is fed serially to the teleprinter mechanism. When the character has been completely transferred, the clock is stopped and the logic reset ready to accept the next data transfer.

2.5.3 Channel Selection

An output to the teleprinter is selected according to the position of the Select Output and/or the type of system in use. (This is accomplished by operating the necessary controls on the Teleprinter and Paper Tape Controller, Figs. C19 and Fig. h refer). For an output to be sent to the teleprinter, TOUT must be true.

If a tape reader and a tape punch are not used, the associated logic is omitted and the READ and PUNCH links on boards 5 and 11 respectively will not be present. This means that the inputs to 14/1B13 and 14/3B11 are always at a true level and will hold TOUT true and POUT false. Under these circumstances the position of the Select Output switch has no effect on the logic and all outputs go to the teleprinter.

When a tape reader and tape punch are used with the system, the READ and PUNCH links will be present. In this case TOUT will be true and POUT false when the Select Output switch is set to TELEPRINTER, or to AUTO with the interface signal [ADDRESS BIT 3] true. At all other times TOUT will be false and POUT true.

2.5.4 Teleprinter Output Timing

2.5.4.1 Data to Register

When data is to be output from the central processor, the interface signal [STP] goes true. This causes $\overline{\text{OUTSEL}}$ to go false and hence T WAIT (the output of 22/3B12) also goes false. With the teleprinter selected, TOUT is true and POUT false, thus T WAIT going false causes $\overline{\text{OUTBUSY}}$ to go true and accept the OUTSEL signal.

The output of 16/1A12 going false sets the bistable 16/4A/4A causing $\overline{\text{ACT}}$ to go false. A 1 μs delay is introduced before $\overline{\text{ACT1}}$ goes false and triggers the monostable 16/5B/4B to produce the 680 ns pulses ACT* and $\overline{\text{ACT*}}$. The 1 μs delay is produced by the capacitor C1 to earth and serves to prevent small spikes propagating spurious ACT* and ACT** pulses. The 680 ns pulse ACT** generated by 16/7B13 sets the bistable 16/2B/2B to send a true [RTR] signal down the interface line.

OUTSEL and TOUT going true causes TDOUT (the output of 15/3B13) to go false. This signal is inverted by 22/4A11 to produce TDOUT. ACT is inverted by 22/4A13 and gated with TDOUT to cause $\overline{\text{RESETL}}$ (the output of 22/1A12) to go false. $\overline{\text{RESETL}}$ is applied to 25/2A12 to prevent the clock from starting until data is transferred to the buffer. The signal applied to 22/4B12 causes $\overline{\text{BLOCK}}$ to go false and this signal inhibits INFO at 23/6A12 and 23/7B11. $\overline{\text{RESETL}}$ inhibits $\overline{\text{ST}}$ signals at 23/7B11.

ACT* is gated with TDOUT at 22/4A12 to produce the 680 ns pulse $\overline{\text{TDOUT*}}$. This pulse sets the bistable 23/3A/3A causing O to go true and $\overline{\text{O}}$ false. $\overline{\text{TDOUT*}}$ is inverted by 19/5A12, 20/7B11 and 21/7B11 and gated with the data signals $\overline{\text{OUT1}}$ and $\overline{\text{OUT8}}$ to transfer the information to the register.

The O signal applied to 23/4A13 causes $\overline{\text{INFO}}$ to be held false and INFO true.

The $\overline{O}$ signal applied to 22/5A12 causes CLEAR to go false and allow data to be entered into the register. $\overline{O}$ applied to 22/4B12 ensures that $\overline{BLOCK}$ remains false and applied to 25/2B12 causes CLOCK BUSY to go true. $\overline{O}$ is also applied to 22/3B13 causing RUN to go true and hence T WAIT to go true.

2.5.4.2 Strobing Register

After the [RTR] signal is received by the central processor, the [STP] signal goes false. This resets the bistables 16/4A/4A and 16/2B/2B in the timing chain and causes $\overline{TDOUT}$ to go true. This is turn causes $\overline{RESETL}$ to go true and the clock is allowed to start. The operation of the clock is described in Section 2.4.5.

The Inputs to 23/7B11 are $\overline{BLOCK}$ which is false, INFO, O and $\overline{RESETL}$ which are true and the output to the teleprinter mechanism is thus controlled by $\overline{ST}$.

With the clock running, the $\overline{S1}$ and $\overline{S2}$ pulses move the data from left to right along the register. The extreme right hand stage has no data input (21/6A13) and this causes $\overline{ST}$ to be false for the first 9.1 ms period. This is used as a Start pulse for the teleprinter mechanism, so that the format of the character is identical to that produced in the input mode of operation. The level of $\overline{ST}$ will subsequently depend on the code of the character output from the processor.

Since INFO is held true and $\overline{INFO}$ false, then each $\overline{S1}$ pulse gates a true and false level respectively into the left hand end of the register. When the character has been completely shifted, the lower output of each stage of the register is at a true level. These outputs are gated in pairs at 21/7B12, 21/7A12, 20/7B12 and 20/7A12 to produce signals $\overline{END\ D}$, $\overline{END\ C}$, $\overline{END\ B}$ and $\overline{END\ A}$ respectively. These four signals with the three stage outputs of

board 19, $\overline{A}$, $\overline{B}$ and $\overline{C}$, are gated together at 19/6A and 19/6B. When all stage outputs are true, END O/P goes true.

END O/P resets the bistable 22/3A/3A causing O to go false and $\overline{O}$ true.

With $\overline{O}$ going true, RUN goes false to prevent further clock pulses. CLEAR goes true to reset the register and $\overline{BLOCK}$ goes true. CLOCK BUSY goes false at the end of the SHIFT pulse to reset the bistable 23/2A/3A as described in Section 2.4.5.

With O going false, $\overline{ST}$ signals are blocked at 23/7B11, and INFO goes false.

The logic is now in a ready state to accept the next data transfer.

2.5.5. Reset Signals

2.5.5.1 $\overline{RESET}$

This signal from 15/7A13 is derived from the [RESET] signal generated in the central processor. The $\overline{RESET}$ signal goes false when the equipment is first switched on and also when the Reset button is operated. The signal remains false until the Jump button is pressed.

The $\overline{RESET}$ signal has four uses:

(1) Applied to bistable 22/1B/1A it ensures that $\overline{L}$ is true.

(2) Applied to bistable 22/3A/3A it ensures that $\overline{O}$ is true.

(3) Applied to 22/2B11 it ensures that the bistable 22/2B/2A is set such that $\overline{R}$ is true.

(4) Applied to 23/6A12 it ensures that INFO is held false.

2.5.5.2 RESET

This is the inverse of RESET and is obtained from 15/7A11. It is applied to 22/5A11 to hold CLEAR true and the register in a reset state.

2.6. Special Clock Circuits

2.6.1. Introduction

The teleprinter clock board DPS14 in position 25 of the logic rack contains two special circuits. Areas D and C each contain a high stability 2.27 ms pulse generator. In Area E is located a stabiliser which provides a +10V d.c. supply for the pulse generators. The remainder of the board contains L.S.A. elements.

The component layout on the board is shown in Fig. C32, together with the circuit diagrams and component tables for the two special circuits.

2.6.2 Pulse Generator

When not in operation the input is held at a false level and VT1 is reverse biased. C1 is not charged and VT2 conducts so that the output presents a false level to the load. When the input goes true, VT1 conducts causing VT2 to be reverse biased and present a true level to the load. C1 charges through R3 and R4 and VT2 again becomes forward bias. The time for this to occur is adjusted on test to a value of 2.27 ms by selecting the value of R3.

2.6.3 Stabiliser

The circuit uses +28V d.c. to produce a +10V d.c. supply with a stability of ± 5% and a regulation of better than 1% for a 30 mA load current.

Changes in the output voltage are sensed by the resistor chain R6, R7 and R8. The value of R6 is selected on test and is wired in parallel with R7 if the output is greater than 10.5V, and in parallel with R8 if the output is less than 9.5V. The sensed voltage controls the bias on VT1, the emitter of this transistor being held at a reference level of 6.8V by Zener Diode MR1. Control of the current through VT1 varies the drive to VT2 and hence the level of the output voltage.

The two transistors are protected from a large reverse bias by diodes MR3 and MR4. The d.c. level on the base of VT2 is prevented from rising above 13V by the Zener diode MR2.

2.7 Maintenance and Test Programs

2.7.1 Maintenance

Details of maintenance and the tools and lubricants required, are as stated in the manufacturer's handbooks. A set of handbooks, tools and lubricants is supplied with each teleprinter.

NOTE: Lifting by diagonally opposite corners and excessive jolting or tilting may upset adjustments. Once installed and set up, the teleprinter should be disturbed as little as possible.

2.7.2 Test Program

A diagnostic program is not provided for the teleprinter. On completion of maintenance checks, the operators daily test program X50 should be run to ensure the correct functioning of the equipment. X50 is described in the Test Program Library Cat. No. MCB 145.

NOTE: In any teleprinter test program a Carriage Return instruction must be followed by a Space or Line Feed instruction. If this procedure is not observed, the teleprinter may attempt to type a character during the carriage return time.

3. ON LINE ADAPTOR FOR PAPER TAPE AND TELEPRINTER CONTROLLER

3.1. Introduction

The On Line Adaptor consists of one logic board which is used to modify the action of the interface timing chain. When the processor attempts to carry out a data transfer and the device required is already busy, the processor is held up until the device is available. In certain circumstances, e.g. tape replacement, the hold up time is undesirable. The On Line Adaptor ensures that in the event of a device being busy, the processor is not held up for longer than 2 μs. If, within 2 μs of a data transfer signal being output from the processor, the device becomes available, then the instruction is carried out normally. If the device remains busy, a pseudo reply is sent to the processor and the control logic is inhibited from making a data transfer.

The On Line Adaptor board also includes a set of lines which indicate the availability of the device and may be used in conjunction with an interrupt scanner.

The board is a type DP4 and is inserted in position 17 of the logic rack.

NOTE: When converting a system for use with an On Line Adaptor, the backwiring link between 16/25 and 16/57 must be removed.

3.2. On Line Operation

The logic diagram of the board is shown in Fig. C33 together with the component details.

With the On Line switch set to ON, a false signal is applied to 14/3B13 causing ON LINE to go true. This signal is inverted by 17/4B13 causing $\overline{\text{ON LINE}}$ to go false.

When an On Line Adaptor is not used, a link is inserted in the backwiring of board 16 and the output of 16/1A12 must go false before the interface timing chain is primed. This condition occurs when the device becomes not busy and the transfer signal is accepted.

When a data transfer is required SELECT goes true. With the On Line Adaptor present and the associated switch set to ON, SELECT and ON LINE being true cause the output of 17/1A13 to go false and trigger the monostable 17/2B/3A. This produces a 2 μs TEST pulse at the end of which, pulse generator 17/3B13 is triggered to produce a 680 ns pulse. This pulse is inverted by 17/3A13 causing $\overline{\text{SET ACT}}$ to go false for 680 ns. The pulse sets the bistable 16/4A/4A to start the interface timing chain and cause [RTR] to go true. The bistable 17/2A/2A is reset by ON LINE such that $\overline{\text{INV}}$ is false. The signal applied to 15/3B13 and 16/4B13 causes the control logic to be inhibited when the interface timing chain signals occur.

If the device becomes available during the 2 μs TEST pulse, the output of 16/1A12 goes false. This signal is inverted by 17/1A11 and then gated with TEST to set the bistable 17/2A/2A causing $\overline{\text{INV}}$ to go true, and remove its inhibit action. $\overline{\text{ON LINE}}$ prevents direct triggering of the timing chain at 17/1A12. $\overline{\text{SET ACT}}$ primes the timing chain at the end of the TEST pulse and a normal data transfer takes place. The bistable 17/2A/2A is reset when SELECT goes false.

3.3 Off Line Operation

If the On Line switch is set to OFF, $\overline{\text{ON LINE}}$ is true. In this case the processor is held up until a device becomes available and the output of 16/1A12 goes false. This signal is inverted by 17/1A11 and gated with $\overline{\text{ON LINE}}$ at 17/1A12. The resultant false signal sets the bistable 16/4A/4A to start the timing chain. ON LINE being false and applied to 17/2A13 ensures that $\overline{\text{INV}}$ is true and the inhibit action is removed. ON LINE also prevents generation of the TEST pulse.

3.4. READY Lines

3.4.1 T/P OUTPUT READY

The signal from 17/5B11 is normally true due to CLOCK BUSY being false and holding the bistable 17/4A/4A in a reset state. When a data output is sent to the teleprinter, CLOCK BUSY goes true and when the ACT** pulse occurs the bistable is set and T/P OUTPUT READY goes false. The false level is maintained until the transfer is completed and CLOCK BUSY goes false.

3.4.2 T/P INPUT READY

The signal $\overline{L}$* applied to bistable 17/5A/5A is normally true so that when the first data transfer occurs and ACT** is produced, the bistable is set such that T/P INPUT READY is false. This condition can only be changed by pressing a key on the teleprinter or starting the printer reader. When the buffer register is loaded $\overline{L}$* goes false to reset the bistable 17/5A/5A causing T/P INPUT READY to go true. After the character has been accepted by the processor $\overline{L}$* goes true and with ACT** sets the bistable again. If a teleprinter output occurs before the character is taken from the buffer register, the character is overwritten by the processor output. $\overline{L}$* goes true and the bistable 17/5A/5A set so that T/P INPUT READY is false.

3.4.3 READER READY

This signal from 17/5B13 is normally true due to R WAIT being false and holding the bistable 17/6A/6A in a reset state. When a data input is required R WAIT goes true and when the ACT** pulse occurs the bistable is set and READER READY goes false. The false level is maintained until the tape is advanced and the buffer register reloaded, R WAIT then goes false.

3.4.4 PUNCH READY

This signal from 17/6B11 is normally true due to P WAIT being false and holding the bistable 17/7A/7A in a reset state. When data is output to the punch, P WAIT goes true and with ACT** sets the bistable causing PUNCH READY to go false. The false level is maintained until punching has been completed and P WAIT goes false.